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Simple Voltage-reference Circuit

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A circuit consisting of three zener diodes and two resistors provides a reference voltage of $\simeq$ 5·3V stable within ±0·3% over a temperature range 0 to 50°C, with mains voltage variations of up to ±10%. Long-term drifts in the components may give a further voltage change of 0·012%.

INTRODUCTION

The Mullard BZY78 is a silicon reference diode with a zener voltage of 5·1 to 5·6V. It has a voltage stability of ±1% at a zener current of 11·5mA±10%, in ambient temperatures between −50 and +100°C. The investigation discussed in this article determined how the voltage stability could be improved by stabilising the zener current and restricting the temperature range.

TEMPERATURE COEFFICIENT

There are two reverse breakdown mechanisms exhibited by semiconductor diodes. Low resistivity material, which has a high level of doping, gives very narrow p-n junctions which break down by internal field emission. The original theory of this form of breakdown is due to Zener, and for this reason all diodes with this characteristic are called zener diodes. In material with a lower level of doping, avalanche breakdown, due to ionisation by collision, will occur at a lower voltage than that required for zener breakdown. Thus, at a specific doping level there is a transition from true zener to avalanche breakdown. This point also depends upon the current density, the junction temperature, and the presence of any impurity in the junction.

The zener breakdown voltage is inversely proportional to the carrier concentration in the higher resistance side of the junction. This concentration increases with junction temperature, giving a negative temperature-coefficient of voltage. Conversely, the avalanche breakdown, which is the effect of ionisation of the valence electrons in the silicon, is critically dependent upon electron mobility, which decreases with a rise in temperature. As a higher voltage must then be developed to maintain the same rate of ionisation, the avalanche mechanism has a positive temperature-coefficient.

Breakdown, which depends upon the current and the junction temperature, may therefore be zener or avalanche or a combination of the two. The BZY78 reference diode operates in the transition region (at about 5·3V) and exhibits high stability with temperature changes.

The coefficient of breakdown voltage with temperature is, for the BZY78, negative at high temperatures (zener) and positive at low temperatures (avalanche). The inversion point varies with current and occurs at higher temperatures as the current is increased. The operating point is selected so that the device operates in the region of high stability with change in temperature, and also has a low slope resistance.

SLOPE RESISTANCE

The slope resistance is defined in terms of a small change in I_z and the associated change in V_z. Thus, as shown in Fig. 1,

$$r_z = \Delta V_z / \Delta I_z.$$

The slope resistance of low-voltage diodes is higher than that of types with breakdown voltages of between 7 and 8V, in which region r_z has a minimum value. Beyond this region the slope resistance increases at a greater rate than the nominal voltage.

The slope resistance also varies with zener current, decreasing exponentially as the current I_z is increased. It is virtually independent of temperature.

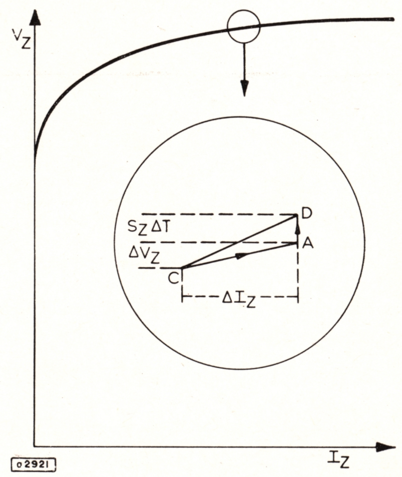

Fig. 1—Dynamic characteristic of zener diode, with small section of curve magnified

The a.c. slope resistance will, in general, be different from the d.c. slope resistance at any point, since a change in dissipation due to d.c. will also change the voltage, unless the temperature coefficient of voltage is zero at that point. In Fig. 1 a change of current ΔI_z produces an instantaneous change of voltage ΔV_z, and the operating point moves from C to A along the dynamic characteristic. The temperature of the device will then change by an amount ΔT because of the increased dissipation, and there is a further change of voltage $S_z \Delta T$, where S_z is the temperature-coefficient of voltage. When thermal stability is achieved, the operating point will have reached D, which is the point that would have been reached by increasing the current very slowly and moving along the line C-D (the static characteristic). Hence the small-signal a.c. slope resistance will be less than the corresponding d.c. value when the temperature-coefficient S_z is positive, and greater than the d.c. value when the coefficient is negative.

The BZY78 has a very low temperature-coefficient of voltage (see *Design*, this page). It may be deduced that the difference between the a.c. and d.c. slope resistance is approximately 0·5Ω. Consider an increase of 1mA in the zener current. The change of power dissipation will be 5·3mW; and, as the maximum thermal resistance is 0·31degC/mW, the junction temperature will increase by 1·64degC. It can be seen, from *Design*, that the maximum resultant change of zener voltage will be

$$\pm(7{\cdot}5/25) \times 1{\cdot}64 = 0{\cdot}49\text{mV}$$

which represents a resistance change of 0·49Ω. This difference between the a.c. and d.c. slope resistance is small compared with 20Ω, which is the nominal dynamic resistance of the BZY78, and it will be neglected.

REFERENCE CIRCUIT

It will be seen that the principal causes of drift in the voltage of a zener diode are changes in reverse current and junction temperature.

Regulation

Each stage of the reference circuit (Fig. 2) may be considered to be a potential divider consisting of a resistor and diode in series, whose regulation is defined as the ratio of the change in output voltage to the associated small change of input voltage. Thus,

$$\text{Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}.$$

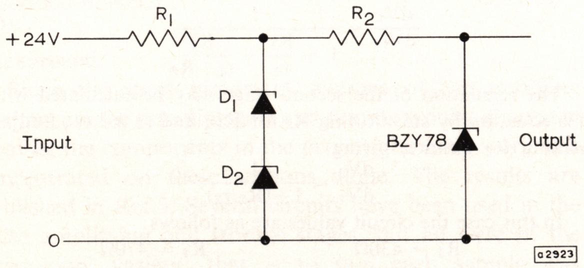

Fig. 2—Reference circuit

An expression is derived in the Appendix (page 292) for the regulation in terms of the source and slope resistances in the circuit, and the overall regulation is the product of the regulations of the successive stages. The reference is designed to be operated from a mains-derived supply which may vary as much as ±10%, therefore the circuit must have good regulation.

Temperature

If the reference is used over the range 0 to 50°C, and standardisation is carried out at room temperature, this interval may be expressed as 25°±25degC. Hence, in the worst case, away from the condition of optimum stability, (the variation of voltage with temperature being approximately linear) this change may be represented by $\pm\Delta V_t$, where ΔV_t is the change in zener voltage over 25degC. At the condition of optimum temperature stability, where the variation is non-linear, ΔV_t will be less than the worst-case value.

The junction temperature will differ from ambient by an amount depending upon the power dissipation in the diode (which may be considered constant) and the thermal resistance. The measurements discussed in this article were made with the devices in a temperature-controlled oilbath. If the diodes are mounted in air, thus increasing the thermal resistance, the temperature difference will be greater, giving a slightly different operating temperature range. For example, if the device is mounted by its leads in free air at a certain temperature, the junction temperature may be up to 10degC higher than when the device is immersed in oil at the same temperature.

Design

The overall regulation improves with the number of stages, but the temperature-coefficient of each stage, although subject to the regulation of succeeding stages, has an adverse effect on the stability. A three-stage reference circuit may be designed to only small advantage, therefore a two-stage circuit is considered in this article.

The first stage must provide an output voltage much greater than 5·3V with a low temperature-coefficient, and it must have good regulation. A suitable output voltage with a low temperature-coefficient may be achieved by using two diodes in series, each with a breakdown voltage of approximately 5V. A very low slope resistance and a high source resistance are necessary (see Appendix) to give good regulation; and so the operating current, and hence the supply voltage, should be high.

Zener diodes from the BZY88-C series were chosen for the first stage. The 5·1V diode type BZY88-C5V1 has a low temperature-coefficient, and two diodes in series give a typical combined voltage of 2×5·35 = 10·7V when run at 20mA, which is high compared with the voltage of the BZY78 (5·3V). At this current it is estimated that each BZY88-C5V1 has a worst-case temperature-coefficient of +0·9mV/degC, and a slope resistance of 10·5Ω. With a 24V supply, which is high compared with 10·7V, and allowing for a zener current of 11·5mA into the BZY78, the values of R_1 and R_2 are 430Ω and 470Ω respectively. The regulation is 0·045 in the first stage and 0·041 in the second, as calculated in the Appendix.

The drift of the BZY78 reference diode was found to be less than ±7·5mV over the range 25°±25degC under conditions of constant drive.

The stability of the reference also depends upon the resistors in the circuit. The variation in resistance value with operating conditions was studied with reference to the Welwyn C22 Panclimatic type, and it was found that the predominant factor was the temperature-coefficient. Self-heating and the voltage coefficient contribute further small variations, giving an estimated total of 0·63% for the resistors in the first stage, and 0·60% in the second.

Calculation

The maximum deviation in the output from each stage may be calculated as follows, using the regulation factors deduced in the Appendix.

First stage:

Supply	$\pm 10\% \times (24 \times 10^3) \times 0{\cdot}045$	$\pm$108mV
Resistor R_1	$\pm 0{\cdot}63\% \times (13{\cdot}3 \times 10^3) \times 0{\cdot}045$	$\pm$ 3·8mV
Diodes D_1, D_2	$\pm 25 \times (2 \times 0{\cdot}9)$	$\pm$ 45mV
Total first stage deviation		$\pm$156·8mV

Second stage:

First stage drift	$\pm 156{\cdot}8 \times 0{\cdot}041$	$\pm$6·43mV
Resistor R_2	$\pm 0{\cdot}60\% \times (5{\cdot}4 \times 10^3) \times 0{\cdot}041$	$\pm$1·33mV
BZY78		$\pm$7·5mV
Total deviation in output		$\pm$15·26mV

This total deviation represents ±0·3% of the minimum nominal reference voltage.

Alternative Design

With a 5·6V diode type BZY88-C5V6 substituted for each BZY88-C5V1, the same overall performance will be obtained if the values of R_1 and R_2 are changed to 390Ω and 530Ω respectively. This design has the advantage of better regulation at the expense of temperature stability; so if it is necessary to use the reference over a wider range of input voltage, this second design is preferable.

Long-term Drift

The reference voltage will be subject to the long-term stability of the resistors and diodes. The resistance values may vary as much as a further 0·15%, and the diodes are subject to a maximum drift of 200μV. These drifts may be in addition to those already calculated, giving a further possible drift of 0·012% from the initial voltage.

APPENDIX

The stage regulation may be calculated with reference to the equivalent circuit, Fig. 3, where

$$V_{in} - V_1 = R_1(i_1 + i_2) \qquad \ldots(1)$$

and

$$V_1 - V_2 = i_2 R_2 . \qquad \ldots(2)$$

From Eqs(1) and (2)

$$V_{in} = V_1 + i_1 R_1 + (V_1 - V_2)(R_1/R_2)$$

or

$$V_1[1 + (R_1/R_2)] = V_{in} - i_1 R_1 + V_2(R_1/R_2)$$

therefore

$$\frac{dV_1}{dV_{in}}\left(1 + \frac{R_1}{R_2}\right) = 1 - R_1 \frac{di_1}{dV_{in}} + \frac{R_1}{R_2} \cdot \frac{dV_2}{dV_{in}} . \qquad \ldots(3)$$

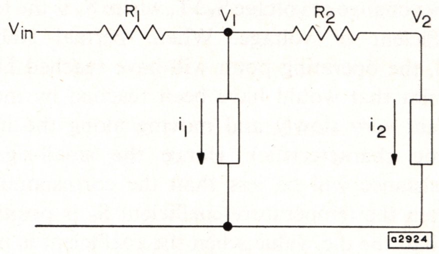

Fig. 3—Equivalent circuit

Now

$$\frac{di_1}{dV_{in}} = \frac{di_1}{dV_1} \cdot \frac{dV_1}{dV_{in}} = \frac{1}{r_1} \cdot \frac{dV_1}{dV_{in}} \qquad \ldots(4)$$

where r_1 is the slope resistance of the first zener voltage at the current i_1.

Also, from Eq(2),

$$V_2 = V_1 - i_2 R_2$$

therefore

$$\frac{dV_2}{dV_{in}} = \frac{dV_1}{dV_{in}} - R_2 \frac{di_2}{dV_{in}}$$

$$= \frac{dV_1}{dV_{in}} - R_2 \frac{di_2}{dV_2} \cdot \frac{dV_2}{dV_{in}} .$$

If r_2 is the slope resistance of the second zener voltage at the current i_2, we have

$$\frac{dV_2}{dV_{in}} = \frac{dV_1}{dV_{in}} - \frac{R_2}{r_2} \cdot \frac{dV_2}{dV_{in}}$$

therefore

$$\frac{dV_2}{dV_{in}} = \frac{1}{1 + (R_2/r_2)} \cdot \frac{dV_1}{dV_{in}}$$

$$= \frac{r_2}{r_2 + R_2} \cdot \frac{dV_1}{dV_{in}} . \qquad \ldots(5)$$

From Eqs(3), (4), and (5)

$$\frac{dV_1}{dV_{in}}\left(1 + \frac{R_1}{R_2}\right) = 1 - \frac{R_1}{r_1} \cdot \frac{dV_1}{dV_{in}} + \frac{R_1}{R_2} \cdot \frac{r_2}{r_2 + R_2} \cdot \frac{dV_1}{dV_{in}}$$

or

$$\frac{dV_1}{dV_{in}}\left(1 + \frac{R_1}{R_2} + \frac{R_1}{r_1} - \frac{R_1}{R_2} \cdot \frac{r_2}{r_2 + R_2}\right) = 1 .$$

Simplifying, we obtain

$$\frac{dV_1}{dV_{in}} = \frac{1}{1 + \dfrac{R_1}{r_1} + \dfrac{R_1}{r_2 + R_2}} . \qquad \ldots(6)$$

The regulation of the second stage may be calculated with this equation by substituting R_2 for R_1, and r_2 for r_1, and by making R_2 infinite, giving

$$\frac{dV_2}{dV_1} = \frac{1}{1 + (R_2/r_2)} . \qquad \ldots(7)$$

In this case the circuit values are as follows:

$R_1 = 430\Omega$ $\quad R_2 = 470\Omega$

$r_1 = 21\Omega$ $\quad r_2 = 20\Omega$.

Then, from Eq(6),

$$\frac{dV_1}{dV_{in}} = 0{\cdot}045$$

and, from Eq(7),

$$\frac{dV_2}{dV_1} = 0{\cdot}041 .$$

Feedback Sampling Channel for Sampling Oscilloscopes

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Mullard Semiconductor Measurement and Application Laboratory

Complete circuit details for the sampling channels of a sampling oscilloscope are given. The feedback system used results in excellent linearity, well-defined gain and a constant bandwidth. The circuit is inexpensive.

INTRODUCTION

The work to be described was the result of an examination of the sampling system used by Chaplin *et al* (Ref.1) with a view to making some improvements which would lead to:

(i) a more reproducible circuit, especially in the probe unit, which used a selected high-frequency alloy junction transistor in the avalanche mode,
(ii) better linearity,
(iii) more accurately defined gain,
(iv) a sampling rate ten times higher (that is, 100kc/s).

The circuits described provide these improvements. They offer an inexpensive means of constructing a complete two-channel sampling oscilloscope of 300 to 500Mc/s bandwidth, using the timebase and trigger circuits already described in Ref.2.

Background

Since the most important sections of the sampling channel are the sampling gate and sampling pulse generator (that is, the components in the probe), the early work was concentrated on these sections alone. The results are published in Ref.3. Several circuits have been used in the pulse amplifying and storage stages, but all were of the 'open-loop' variety; that is to say, each sample was treated separately and hence the overall transfer characteristic was the product of the separate characteristics, most of which were non-linear. Consequently, all waveforms of appreciable amplitude were displayed with an intolerable degree of amplitude distortion. In addition, the overall effective gain of the channel tended to change over quite short periods of time. These effects meant that graticule calibration of sensitivity was impossible.

Furthermore, the bandwidth was a function of the instantaneous signal amplitude or the vertical positioning bias or both, a state which is obviously undesirable. This was because of the non-rectangular shape of the sampling pulse (see Ref.3).

Another disadvantage of the open-loop system is that the output waveform is not a continuous analogue of the input, but has a 'boxcar' shape; that is, a series of long pulses having varying amplitude but a fixed baseline, as in Fig. 1. This leads to complications in later amplifying stages (for example, c.r.t. deflection), since these must have sufficient bandwidth to preserve the sharp reset pulses and thus keep the trace blanking period to a minimum, even though the frequency components of the transformed signal may be quite low (d.c. to 100kc/s).

The question soon arose, 'Can negative feedback be applied to a sampling channel to improve overall performance?' Simply feeding the inverted output waveform back to the probe input would obviously not help, since each sample is taken independently of the previous one: the integrator is reset to zero at each sample. However, by storing the 'previous' sample, and feeding this back to the sampling gate, the effective input to the gate becomes the difference in amplitude between two adjacent points on the sampled waveform. The system will then automatically seek a balance point, when the output of the storage circuit is exactly equal to the input voltage. That this principle could be realised was made evident by the appearance of an oscilloscope described in Ref.4. This marked an important step forward by using such a closed-loop system to achieve a bandwidth of d.c. to 500Mc/s (later 800Mc/s, and recently 3000Mc/s) on two identical channels. The closed-loop principle had, of course, been used in sampling systems for some time (Ref.5), but not at such wide bandwidths. Since this instrument was introduced, closed-loop systems have been used almost exclusively.

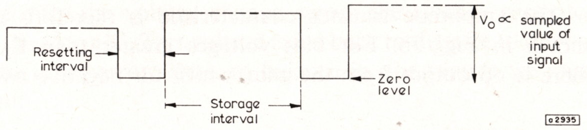

Fig. 1—Open-loop 'boxcar' display

Prevalent sampling circuits are symmetrical; that is, the input error is sensed for both magnitude and sign. Since a great deal of time had already been spent on the 'single-sided' open-loop systems, it was decided to attempt the construction of an asymmetrical closed-loop system. In this system the error signal from the sampling gate is always 'positive', and some mean value of this signal corresponds to the balance input. A positive error at the input to the gate increases the magnitude of error pulse, whereas a negative input error decreases the magnitude.

The method is quite successful, but a 'single-sided' system is not recommended in general, for reasons that are explained later. However, it has one important advantage, which is that the sampling gate has to use only one non-linear element, usually a semiconductor diode. A symmetrical system must use at least two diodes, and more usually four, which raises some problems of driving and matching. Further, there are several experimental gates already in operation which have very wide bandwidths but use a single diode, often mounted in a coaxial cavity, and the output of these is applied to a simple open-loop system. It should be possible to improve the performance of such gates with a single-sided closed-loop system.

BASIC SINGLE-SIDED SAMPLER

The block diagram of the basic system is shown in Fig. 2, but first let us consider the idealised single-diode gate shown in Fig. 3a. We are interested in the form of the amplitude transfer characteristic. If the sampling pulse is perfectly rectangular, the diode ideal, and the load purely resistive, it can be seen that the charge contained in the output pulse is

$$\frac{(E_p - E_B)\tau}{R_L} \qquad \ldots(1)$$

where

E_p is the amplitude of the sampling pulse
E_B is the bias voltage
τ is the duration of the pulse
and R_L is the load resistance.

The amplitude transfer characteristic is therefore as shown in Fig. 3b. For bias voltages greater than E_p, there is no output from the gate, whilst for negative bias voltages ($E_B < 0$), there is no further increase in the pulsating part of the load current, and so the gate saturates.

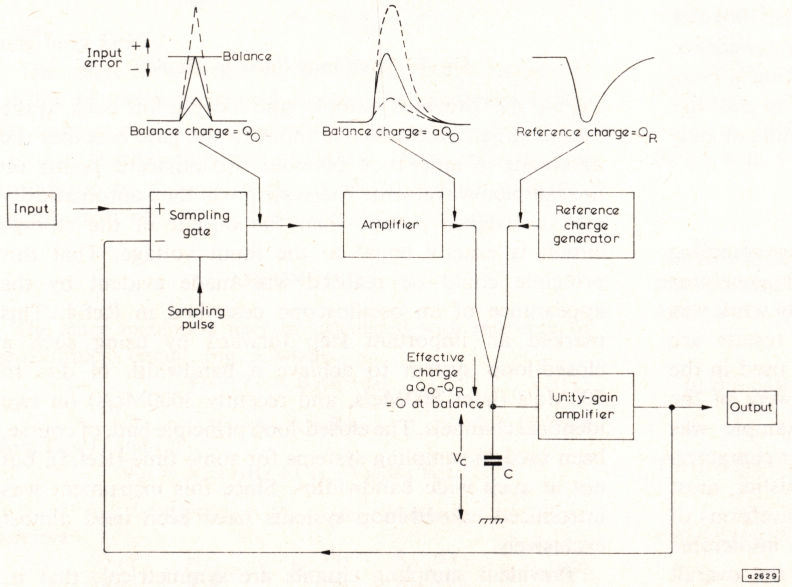

Fig. 2—Basic single-sided sampler

Now, the input signal is effectively added to the bias voltage, so that for equal signal-handling capacity above and below the working-point, the bias voltage would be chosen as $E_p/2$. However, wherever the working point is placed between $E_B = 0$ and $E_B = E_p$, both the slope, $\Delta Q/\Delta E_B$, and the bandwidth are constant. Note that the transfer slope has the dimensions of capacitance, and in this case is

$$S_T = \frac{Q_{max} - Q_{min}}{E_{B(max)} - E_{B(min)}} = \frac{(E_p\tau/R_L) - 0}{E_p - 0} = \frac{\tau}{R_L} \qquad \ldots(2)$$

With reference, now, to Fig. 2, assume that the effective bias voltage is developed across the two terminals marked + and − on the sampling gate, and assume also that the input is initially set to zero. The amplifier output is applied to the storage capacitor C, also charged by the 'reference charge generator', which produces a pulse of opposite polarity to the amplifier at each sampling time. Thus, the charge input Q_i to the capacitor is given by

$$Q_i = aQ_o - Q_R \qquad \ldots(3)$$

where a = amplifier gain
Q_o = gate output
Q_R = reference charge.

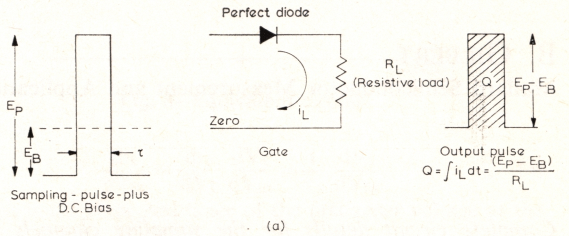

Fig. 3a—Idealised gate

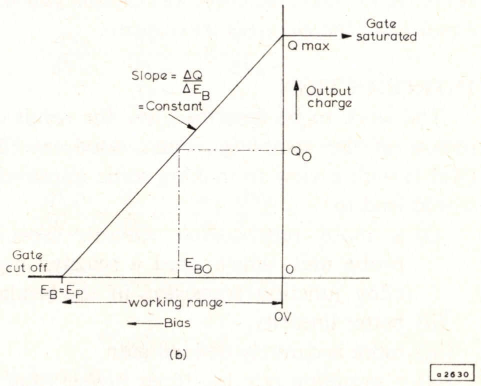

Fig. 3b—Idealised transfer characteristic

As long as aQ_o and Q_R are unequal, the voltage on the capacitor changes, until the bias voltage reaches a value such that $aQ_o = Q_R$, at which point the system is 'balanced'. If the input voltage is changed, let us say to a positive value, the gate output increases, causing V_c to rise until balance is restored.

It is evident that three conditions need to be examined more closely: first, the value of amplifier gain necessary to cause the system to balance in one sample; second, the size of the reference charge; and third, the method of determining the magnitude of C. These points are discussed below.

Storage Capacitor

The capacitor, C, acts as a storage element for the value of the last sampled point on the input waveform. Since the interval between samples may be several tens of milliseconds (that is, when the waveform recurs at a rate below 100c/s), a large value of capacitance is desirable, to offset the effects of inevitable leakage currents. On the other hand, a short charging time (< 1μs) must be used if the system is to work at repetition rates up to about 100kc/s. The capacitance is also partly determined by the actual voltage limits of the storage circuit.

As a practical example, we can calculate the capacitance by two methods, one which ensures that leakage has negligible effect, and the other which ensures that the capacitor can be charged through the full 'window' by a single pulse from the amplifier.

Leakages in the capacitor will be about 2 to 5nA, and the store window about 10V. Assume that the noise-level of the probe is one-thousandth of the full window voltage; referred to the store this amounts to 10mV. We can tolerate about the same amount of droop between samples as noise. Finally, assume the maximum interval is to be 100ms. Then

$$\frac{2 \times 10^{-9} \times 10^{-1}}{10^{-2}} \leqslant C \leqslant \frac{5 \times 10^{-9} \times 10^{-1}}{10^{-2}}$$

therefore

$$C = 20 \text{ to } 50\text{nF}.$$

For the other estimate, assume we have 1μs in which to fully charge the capacitor through 10V, and the amplifier output pulse is roughly triangular in shape, having a maximum amplitude of 50mA. The charge in the pulse is therefore

$$\tfrac{1}{2} \times 10^{-6} \times 50 \times 10^{-3} \text{ coulombs} = 25\text{nC}.$$

Therefore

$$C = \frac{25 \times 10^{-9}}{10} = 2{\cdot}5\text{nF}.$$

The capacitor should therefore have a value somewhere between 2·5nF and 50nF, and a compromise value of 10nF is chosen, which means that the maximum droop could be about 20 to 50mV and that the maximum single step amplitude at the store can be 2·5V. The second result might be of importance when the system is working at low sampling densities and high signal amplitudes, but normally the difference between samples will not exceed this value, and furthermore a compensating circuit is included to reduce the possibility of sampling lag.

Amplifier Gain

The amplifier gain can now be calculated. It will first be shown that the loop gain must be unity if the system is to rebalance exactly at each sample.

Assume that the input has just undergone a step change of amplitude. (Such a step occurs as the sampling sweep returns to the starting point if the initial and final value of the displayed waveform are unequal.) Also assume that the step is of unit magnitude, and that the loop gain is A. During the period following the change, but before the next sample, the output is held at the value of the input before the change; that is, there is an output error of unit magnitude, and therefore an input error of unit magnitude. When the next sample is taken, the output excursion is A volts, leaving an error of $1-A$ to be corrected at the next sample. The output at the next sample will thus be $A+A(1-A)$ and the remaining error $1-[A+A(1-A)]$. It can be seen that the error remaining after n samples is $(1-A)^n$. For no error after one sample, A must be unity.

When $A < 1$, there is an apparent rise-time to the waveform (Waveform 20)*, and when $A > 1$ there is apparent 'ringing' (Waveforms 18 and 19)*. The latter case is undesirable for obvious reasons. However, the case where $A < 1$ can be useful since any noise generated inside the loop, or on the input signal itself, or any apparent noise due to timing jitter on transitions, is reduced in proportion to the reduction in gain.

Now for a small error voltage Δv at the input to the gate, the output charge at sampling will be $S_T.\Delta v$. The output from the pulse amplifier is therefore $S_T.\Delta v.a$, where a is the charge gain of the amplifier. (This assumes that all of the gate output reaches the amplifier.) Consequently the voltage change across the storage capacitor is $S_T.\Delta v.a/C$. This voltage is fed back to the gate to oppose the input error; thus, to balance in one sample we must put

$$S_T.\Delta v.\frac{a}{C} = \Delta v$$

$$a \doteq \frac{C}{S_T} = \frac{C.R_L}{\tau}. \qquad \ldots(4)$$

If typical values are inserted, such as

$$C = 10\text{nF}$$
$$R_L = 100\Omega$$
$$\tau = 5 \times 10^{-10}\text{s}$$

then $$a = \frac{10^{-8} \times 100}{5 \times 10^{-10}} = 2000 \text{ times.}$$

An experimental amplifier might provide for variable gain between 500 and 10 000.

Reference Charge

Strictly speaking, the reference charge, Q_R, which is required to complete the system is now determined solely by the operating point at which the gate is to operate, as the following explanation will show.

The system balances when

$$aQ_o = Q_R.$$

Now, from Eq.(1)

$$Q_o = \frac{\tau}{R_L}(E_p - E_B)$$
$$= S_T(E_p - E_B)$$

therefore

$$aS_T(E_p - E_B) = Q_R \qquad \ldots(5)$$

therefore

$$E_B = E_p - \frac{Q_R}{aS_T}. \qquad \ldots(6)$$

Thus, as Q_R is increased the bias voltage decreases and the working point shifts towards the 'saturated' end of the transfer characteristic. From Fig. 3b, it is seen that the ideal working point is $E_{BO} = E_p/2$. With the values

---

*Waveform notation is given in Appendix 2.

$a = 2000$ times
$S_T = 5 \times 10^{-12}$ coulombs/volt
$E_p = 4V$

then

$$Q_R = 2000 \times 5 \times 10^{-12}\left(4 - \frac{4}{2}\right) = 20\text{nC}.$$

It will be noted from page 295 that the typical maximum charge available from the amplifier is 25nC. It would not be possible, therefore, for it to supply a mean output of 20nC to balance Q_R, so Q_R is calculated to be approximately a half of the maximum capability of the amplifier, and the values for a and C readjusted.

NON-LINEARITY IN THE SAMPLING GATE

The sampling pulse in a practical gate is far from rectangular. (If it were it would be reduced in width until only the rise and fall remained, thus increasing the bandwidth as much as possible.) Fig. 4 shows a typical sampling pulse waveform. The diode also is imperfect. It has capacitance, which means that current flows in the load before the diode is forward-biased; it exhibits forward recovery, which persists during the whole of the forward conduction period in this case, and prevents the loop current from rising to its theoretical value; current carriers injected during the forward conduction phase continue to flow after the diode is reverse-biased, leading to a delayed switch-off. These effects are sketched in Fig. 4 for two different bias levels.

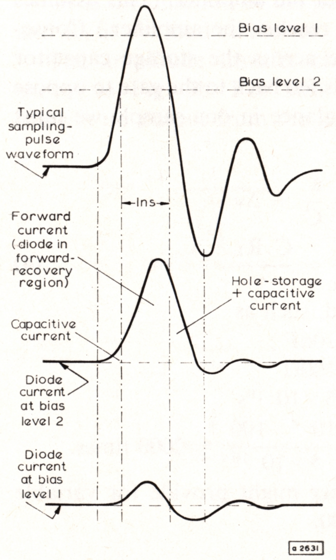

Fig. 4—Departure of diode current from ideal rectangular form

The overall result of these effects, added to the normal non-linearly-resistive character of the diode, is a non-linear transfer characteristic which considerably complicates the design of the system.

Fig. 5 shows a typical transfer characteristic, along with a curve showing the variation in bandwidth with bias point.

The central portion of the curve is reasonably linear, and one might choose a working point such as $E_{BO(2)}$, thus giving equal signal capacity in both positive and negative directions. However, this may not provide adequate bandwidth, and an alternative point using a bias of $E_{BO(1)}$ would increase the bandwidth considerably.

A further difficulty is that the transfer slope, S_T, is no longer constant, but is a function of E_B. The loop gain can therefore be unity at one point only (nominally the chosen working point). On abrupt changes in the input signal, the loop gain rises or falls for one or two samples, and this effect becomes more severe as the input signal amplitude approaches the maximum permissible value. Thus, a high-amplitude pulse might be displayed as shown in Fig. 6.

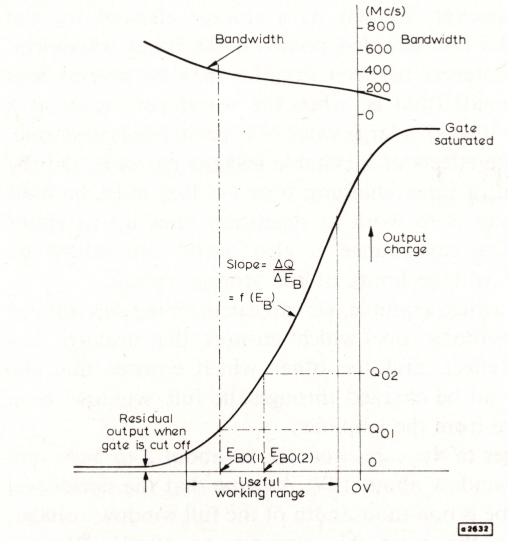

Fig. 5—Practical transfer characteristic and bandwidth curve

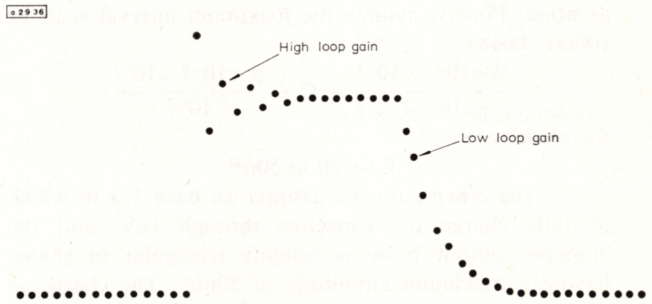

Fig. 6—High amplitude pulse display

This effect can be minimised by (i) introducing non-linearity of opposite shape into the amplifier Q_{OUT}/Q_{IN} characteristic, (ii) making Q_R a function of the error pulse amplitude, so that error signals above the mean amplitude increase Q_R and vice versa.

Both methods have been tried, and the latter seems easier to incorporate into a practical instrument. The details are given on page 300.

COMPLETE PRACTICAL SYSTEM

A block diagram of a practical system is shown in Fig. 7. The input signal is applied to the gate via a times-five attenuator which serves both to decrease the input admittance and increase the signal capacity. This benefit is obtained at the expense of the noise level referred to the input.

The output charge from the gate is first amplified by a low-noise pre-amplifier which has provision for varying the gain. The amplified pulse is passed through the stability gate which opens for approximately 0·5μs after each sample. This gate prevents continuous oscillation around the loop which might occur via a feedback path in the pre-amplifier (through R_{102} of Fig. 11). An output amplifier raises the power level to a value sufficient to operate the store.

The reference-charge generator is driven by a pulse from the timing circuits (Ref.2), but there is additional drive from the output amplifier which modulates the reference charge according to the pulse amplitude.

The store consists of two silicon diodes, a polystyrene capacitor and a cathode-follower; the output is applied to a times-ten amplifier. The amplified output signal is passed to a buffer cathode-follower.

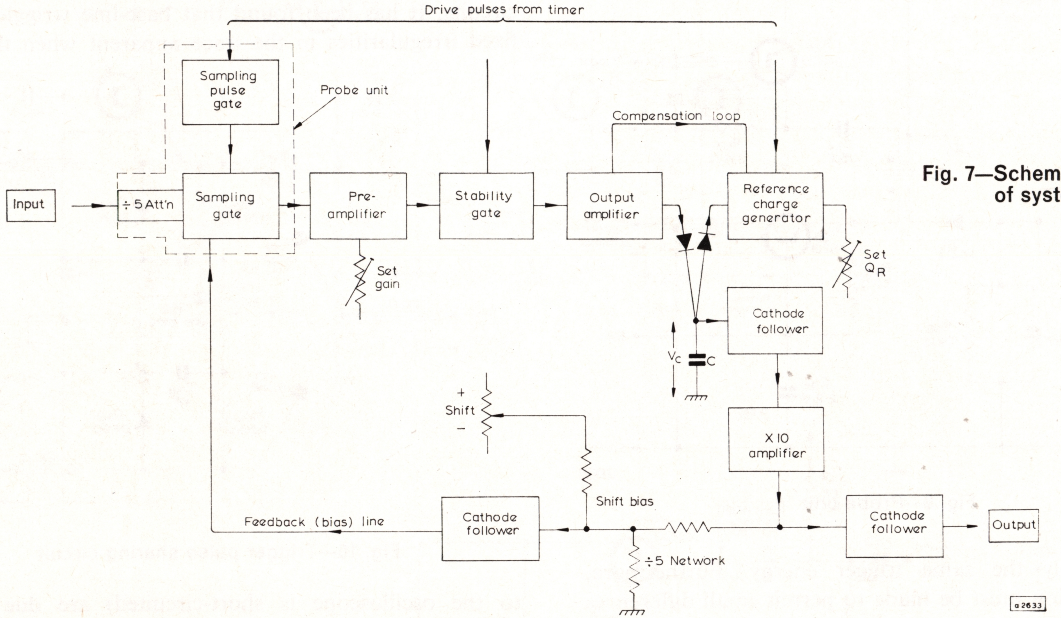

Fig. 7—Schematic diagram of system chosen

One-fifth of the output signal is then returned to the sampling gate, via a cathode-follower, and added to a shift bias voltage. Thus the effective overall gain is determined by the feedback attenuator and the input attenuator; and since these both have gain factors of five, the overall gain is unity.

The non-linearity introduced by the two cathode-followers, the only active links in the chain between output and input, is negligible, since they have very long current tails and are working 'back-to-back'.

It is important to notice the effect of introducing a shift bias into the feedback line. The bias at which the gate operates is the voltage difference between the input voltage (after attenuation) and the feedback voltage. This bias must satisfy the condition for loop balance as stated in Eq.(6); any change at the input is followed by the output voltage to restore this balance. Similarly, any out-of-balance voltage on the feedback line is offset by a change of output voltage, so that if the input terminal of the probe is earthed, the input to the feedback cathode-follower is constant, whatever the setting of the shift bias control, provided that the rest of the system (store and post-store amplifiers) is still within its operating range.

The main function of the shift bias is, of course, to keep the system within its operating range for a wide range of pedestal voltages at the input. Its secondary function is to position the trace.

Two-channel System

Two or more channels can be operated together from common timing circuits. The circuits described assume that two channels are required. Interconnection is straightforward and is shown in Fig. 8.

PROBE

The probe, which contains the sampling-gate, a common-base amplifier and the sampling-pulse generator, has been described in Ref. 3.

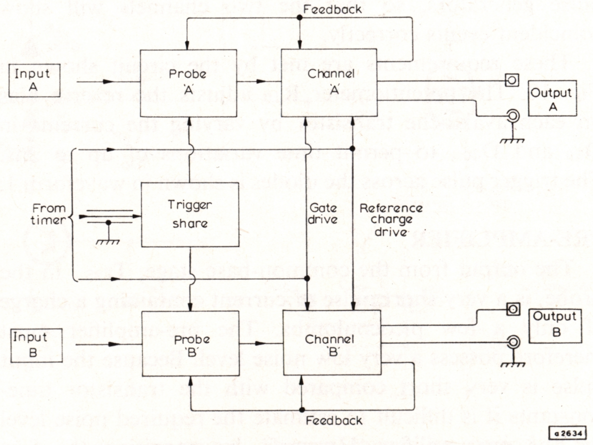

Fig. 8—Interconnection of two channels

Experience with small quantity production of these probes has resulted in some doubt concerning the ease of attaining the performance figures quoted in the above reference. The bandwidth of some probes falls to the region of 300 to 500Mc/s, which is considerably less than that measured on prototypes. The reason for this is not fully understood, but it seems likely that small changes in the layout coupled with less favourable triggering conditions for the sampling-pulse generator could explain the loss.

Also, the resistor values in the attenuator have been reduced to give an input resistance of 50kΩ. This slightly reduces the noise level, possibly because the effects of small fluctuations in the leakage current of the sampling diode are reduced. The probe is shown in Fig. 9.

Trigger Pulse Sharing

When two probes are operated from a single trigger source, the pulse must be applied to both probes through a sharing circuit, which ensures that each probe receives approximately the same trigger energy. Furthermore, some provision must be made to permit small differences to be taken up in the firing times of the two sampling-pulse generators, so that the two channels will show coincident events correctly.

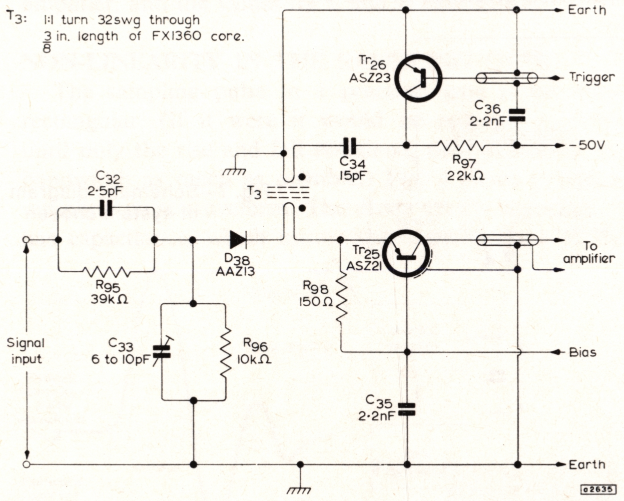
T$_3$: 1:1 turn 32swg through $\frac{3}{8}$ in. length of FX1360 core.
Earth
Tr$_{26}$ ASZ23
Trigger
C$_{36}$ 2·2nF
−50V
C$_{34}$ 15pF
R$_{97}$ 22kΩ
C$_{32}$ 2·5pF
T$_3$
R$_{95}$ 39kΩ
D$_{38}$ AAZ13
Tr$_{25}$ ASZ21
To amplifier
R$_{98}$ 150Ω
Signal input
C$_{33}$ 6 to 10pF
R$_{96}$ 10kΩ
Bias
C$_{35}$ 2·2nF
Earth
a2635

Fig. 9—Probe unit

These requirements are met by the circuit shown in Fig. 10. The potentiometer R$_{10}$ adjusts the reverse bias on each avalanche transistor by varying the currents in D$_{39}$ and D$_{40}$, to permit time variations of up to 2ns. The trigger pulse across the diodes is shown in waveform 1.

PRE-AMPLIFIER

The output from the common-base stage, Tr$_{25}$, in the probe, is a very short pulse of current containing a charge of only a few picocoulombs. The pre-amplifier must therefore possess a very low noise level. Because the input pulse is very short compared with the transistor time-constants it is difficult to estimate the required noise level for the pre-amplifier. However, by operating the first transistor at a low collector voltage and current (−5V, 0·77mA), and by taking precautions against stray pick-up etc., it has been found that very little of the noise present on the final displayed waveform is the result of noise originating in the pre-amplifier. The d.c. analysis is given in Appendix 1. The d.c. voltages shown on the diagrams in this article are those indicated when a 10MΩ valve-voltmeter is used.

Pulse-stretching

It was originally proposed to use fast transistors in the amplifier with additional passive components added to introduce controllable stretching. It was found experimentally, however, that the transistor time-constants themselves could be used to produce the desired degree of stretching.

Gain Control

The charge gain of the amplifier can be adjusted by alteration of the external emitter impedance of Tr$_{28}$ (Fig. 11). This is implemented by means of R$_{11}$.

Decoupling

Careful decoupling is essential in the pre-amplifier circuits. It has been found that base-line wriggles (small fixed irregularities in the trace apparent when the input to the oscilloscope is short-circuited) are due almost entirely to miscellaneous disturbances on supply lines, originating in the early stages of the timing circuits. By careful attention to screening, layout and decoupling the amplitude of these irregularities can be reduced to that of the level of other noise.

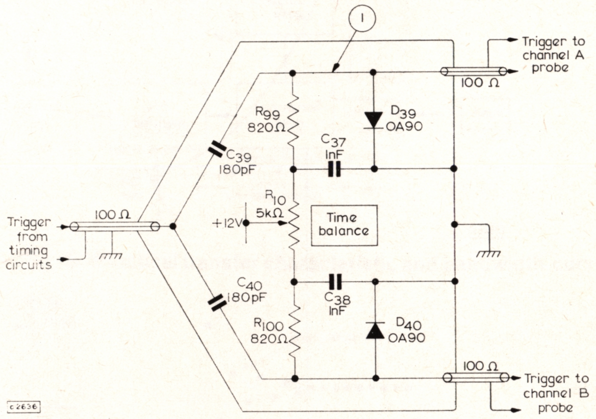
1
Trigger to channel A probe
100 Ω
R$_{99}$ 820Ω
D$_{39}$ OA90
C$_{37}$ 1nF
C$_{39}$ 180pF
R$_{10}$ 5kΩ
+12V
Time balance
Trigger from timing circuits
100 Ω
C$_{40}$ 180pF
C$_{38}$ 1nF
R$_{100}$ 820Ω
D$_{40}$ OA90
100 Ω
Trigger to channel B probe
c2636

Fig. 10—Trigger pulse sharing circuit

STABILITY GATE

The stability gate consists of the two transistors Tr$_{29}$ and Tr$_{30}$ shown in Fig. 11. During intervals between samples, Tr$_{29}$ base is held at −0·3V, whilst Tr$_{30}$ base is earthed. Thus, any output current from Tr$_{28}$ which does not flow in R$_{108}$ flows into Tr$_{29}$ and is diverted out of the loop. During the 'active' period, the base of Tr$_{29}$ rises to +0·8V for 0·5μs, placing Tr$_{30}$ in a slightly conducting state. Its collector current during this initial period causes a small pedestal pulse of current at the collector of Tr$_{30}$. This pulse is of no great consequence; it effectively subtracts from the reference charge magnitude. As the d.c. analysis in Appendix 1 shows, the magnitude of this pedestal varies from −0·82mA to 1·133mA, which are the worst case limits for the stated component spreads. The negative value means that the amplifier output must not exceed this current before Tr$_{30}$ switches on. However, a statistical analysis using a Monte Carlo method shows that approximately 95% of all circuits constructed will give a pedestal current between 0·00 and 0·50mA, and hence a pre-set control for R$_{108}$ is not justified.

The amplified pulse is of mean amplitude 7·5mA and turns Tr$_{30}$ fully on and thus drives the output amplifier. Tr$_{30}$ is turned off after 0·5μs by the gating pulse on Tr$_{29}$ base, so that any part of the amplified pulse after this time is chopped off. This implies that the gating duration must be stable, since small variations in it lead to the introduction of an effective noise component. In the worst case, where the amplifier output is still at maximum amplitude when chopped, a jitter of one part in 1000 in the 0·5μs pulse would lead to about 10mV of noise at the input. However, as waveform 15 shows, the output current falls below the quiescent value after 0·2μs, so that jitter on the gating pulse does not contribute toward the noise level of the system. Waveform 16 shows the output current of the amplifier for positive and negative error inputs. Waveforms at various other points in this circuit are shown in 2, 3 and 4.

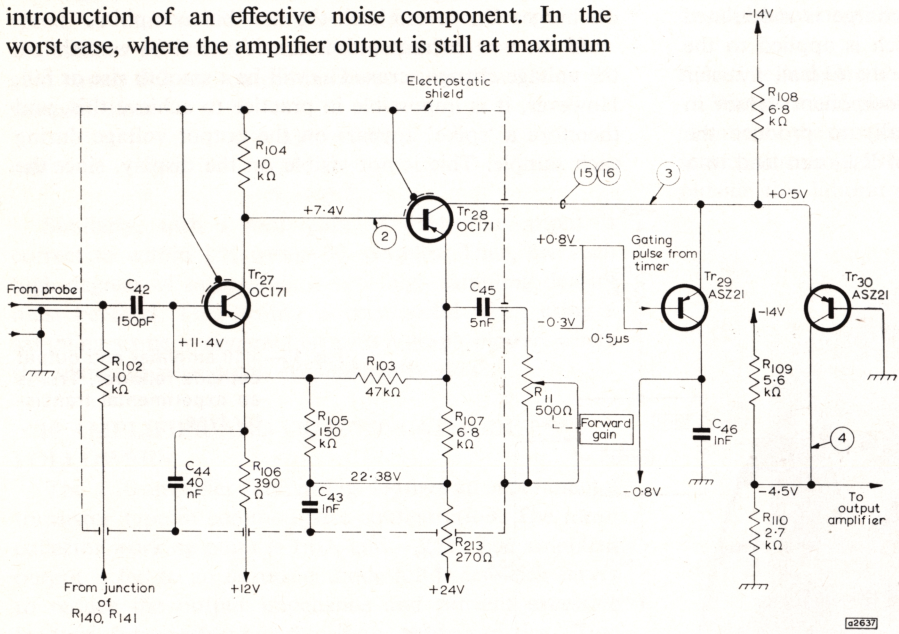
Electrostatic shield
−14V
R$_{108}$ 6·8 kΩ
R$_{104}$ 10 kΩ
15
16
3
+0·5V
+7·4V
2
Tr$_{28}$ OC171
+0·8V
Gating pulse from timer
From probe
C$_{42}$ 150pF
Tr$_{27}$ OC171
C$_{45}$ 5nF
−0·3V
0·5μs
Tr$_{29}$ ASZ21
−14V
Tr$_{30}$ ASZ21
+11·4V
R$_{102}$ 10 kΩ
R$_{103}$ 47kΩ
R$_{11}$ 500Ω
R$_{109}$ 5·6 kΩ
R$_{105}$ 150 kΩ
R$_{107}$ 6·8 kΩ
Forward gain
C$_{46}$ 1nF
4
C$_{44}$ 40 nF
R$_{106}$ 390 Ω
22·38V
C$_{43}$ 1nF
−0·8V
−4·5V
To output amplifier
R$_{110}$ 2·7 kΩ
R$_{213}$ 270Ω
From junction of R$_{140}$, R$_{141}$
+12V
+24V
a2637

Fig. 11—Pre-amplifier and stability gate

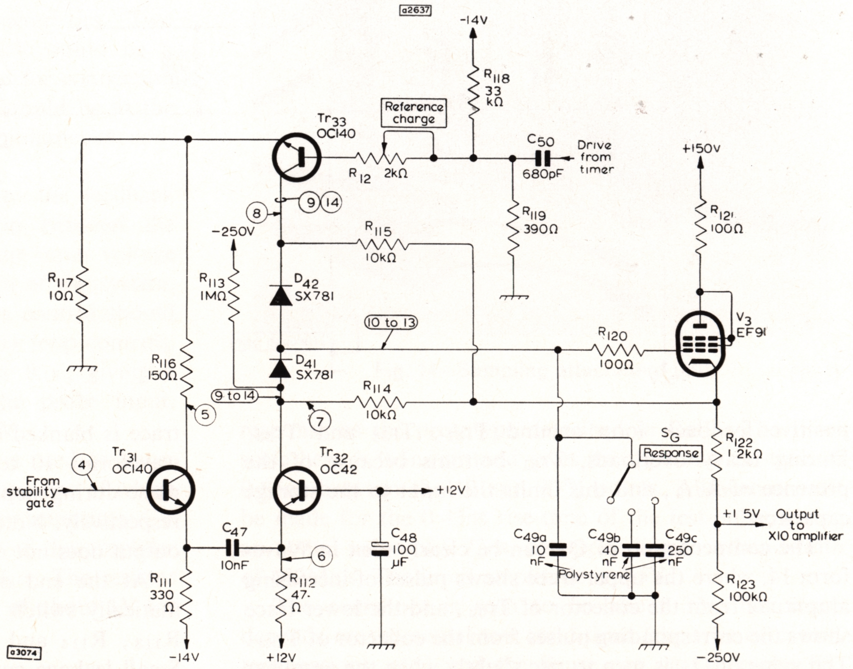
−14V
R$_{118}$ 33 kΩ
Tr$_{33}$ OC140
Reference charge
R$_{12}$ 2kΩ
C$_{50}$ 680pF
Drive from timer
+150V
8
9
14
−250V
R$_{115}$ 10kΩ
R$_{119}$ 390Ω
R$_{121}$ 100Ω
R$_{117}$ 10Ω
R$_{113}$ 1MΩ
D$_{42}$ SX781
10 to 13
V$_3$ EF91
R$_{120}$ 100Ω
R$_{116}$ 150Ω
D$_{41}$ SX781
9 to 14
R$_{114}$ 10kΩ
5
7
S$_G$
Response
R$_{122}$ 1·2kΩ
4
From stability gate
Tr$_{31}$ OC140
Tr$_{32}$ OC42
+12V
+1·5V
Output to X10 amplifier
C$_{47}$ 10nF
6
C$_{48}$ 100 μF
C$_{49a}$ 10 nF
C$_{49b}$ 40 nF
C$_{49c}$ 250 nF
Polystyrene
R$_{111}$ 330 Ω
R$_{112}$ 47 Ω
R$_{123}$ 100kΩ
a3074
−14V
+12V
−250V

Fig. 12—Output stage of amplifier with signal storage gate and cathode follower

OUTPUT AMPLIFIER

The current pulse from Tr$_{30}$ is of insufficient amplitude and charge to drive the storage circuit efficiently. A final amplifier consisting of an emitter-follower and a common base output stage is used to raise the power level in the error pulse. This is shown in Fig. 12. An n-p-n transistor is used for the emitter follower, since the drive at this point is positive-going. During the pulse period, C$_{47}$ charges through about 1V; a large tail current in R$_{111}$ ensures complete discharging of C$_{47}$ within the 10μs (minimum) cycle time.

The output pulse from the collector of Tr$_{32}$ is of approximately 10mA amplitude and 1μs duration, and has a mean charge of 7nC (see Waveforms 5 to 9; Waveform 9 shows collector current of both Tr$_{32}$ and Tr$_{33}$ at balance. Equal areas are evident).

REFERENCE CHARGE GENERATOR

Tr$_{33}$ produces a pulse current of the opposite polarity and approximately the same waveshape and amplitude as the amplifier output. It is driven by a pulse from the timing circuits, and the amplitude can be adjusted to give a charge up to about 20nC by varying the drive with R$_{12}$.

Compensation Loop

The magnitude of the reference charge is modulated by the error pulse, a portion of which is applied to the emitter of Tr$_{33}$. This tends to linearise the overall transfer characteristic inside the loop. The component values in this circuit were chosen experimentally to produce the best compromise. Too high a value of R$_{117}$ can lead to a positive feedback loop around Tr$_{31}$, Tr$_{32}$ and Tr$_{33}$. During heavy overloads, Tr$_{31}$ bottoms because of the presence of R$_{116}$, and this limits the input to the storage capacitor.

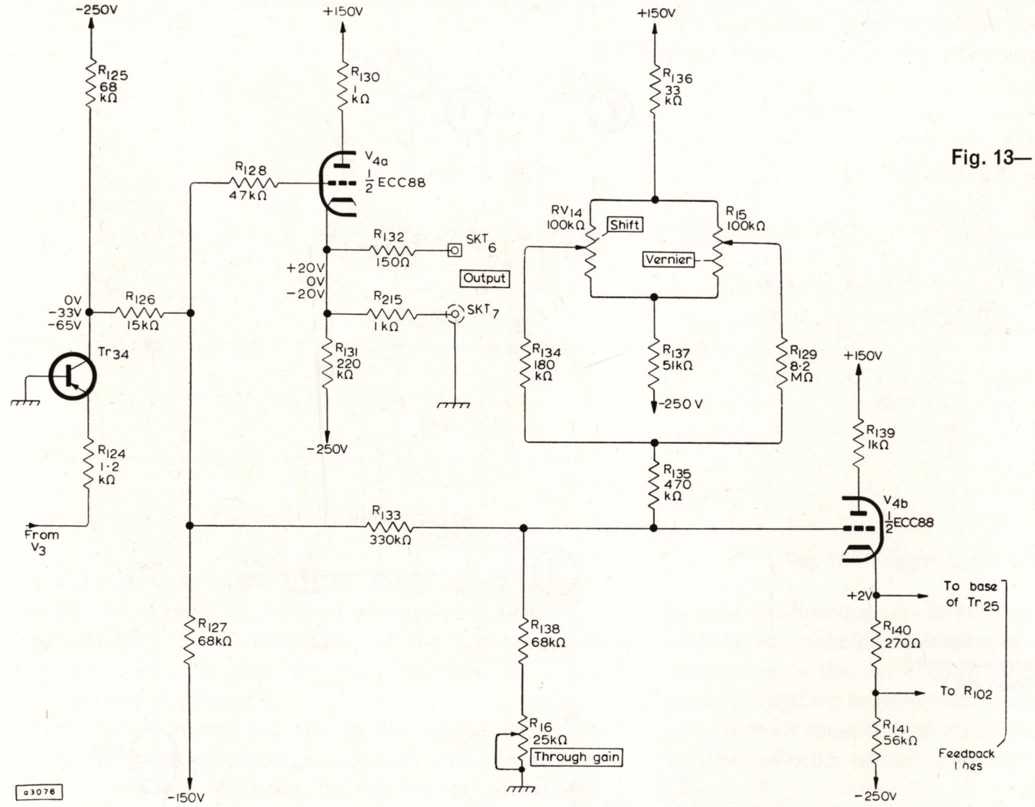

Fig. 13—×10 amplifier and output cathode follower. Tr$_{34}$ is an experimental transistor type

The compensation of Q$_R$ can be clearly seen in Waveform 14, where the upper trace shows pulses of increasing amplitude from the collector of Tr$_{32}$, and the lower trace shows the corresponding pulses from the collector of Tr$_{33}$. The value of Q$_R$ is seen to rise slightly when the amplifier output rises, and the variation shown is sufficient to make the transfer characteristic linear to the required degree.

STORAGE GATE AND CATHODE FOLLOWER

D.C. Considerations

The 'window' of the store extends from about +1V, when D$_{42}$ is nearly forward-biased, to about +11V, when D$_{41}$ is nearly forward-biased. The mean working point is thus +6V at the grid of V$_3$, or about +8V at the cathode. D$_{41}$ and D$_{42}$ are thus normally reverse-biased by 2V, and the bootstrap connection ensures that this hold-off voltage is independent of the value of voltage stored in C$_{49}$.

Operation

During the sampling interval, D$_{41}$ is forward-biased by the pulse from Tr$_{32}$, and D$_{42}$ is forward-biased by the pulse from Tr$_{33}$. The difference-current charges or discharges C$_{49}$ to establish the new balance point.

If the two current pulses are identical in waveshape, the voltage change across C$_{49}$ will be a smooth rise or fall. However, it is impossible in practice to achieve this, and therefore a 'spike' appears on the output voltage during each sample. This is not visible on the display, since the trace is blanked during this period, but it can be seen in waveforms 10 to 13, which show the amplifier output pulse during step changes of +1V, −1V, +5V and −5V respectively. Note that in the last two cases, the amplifier output does not immediately return to its quiescent value.

At the end of the pulsing period, the diodes automatically switch off, as a result of the bias voltages via R$_{113}$, R$_{114}$ and R$_{115}$. The capacitor is thus isolated. Small leakage currents in the diodes and grid current in V$_3$ cause the voltage on the capacitor to drift slightly; but as was shown earlier, the effect is slight above a sampling rate of 10c/s.

Response Control

The switch S$_G$ permits extra capacitors to be switched across C$_{49}$. This simply reduces loop gain since, from Eq.(4), Loop gain = S$_{Ta}$/C. The stated values give nominal loop gain values of 1·0, 0·2 or 0·04. With the loop gain less than unity the effective noise level is reduced by a factor of 5 or 25 in these examples. The actual improvement achieved, however, is not quite so good as theory predicts, partly because of the presence of base line disturbances, and because of noise introduced after the sampling loop, and also because of the spectral distribution of the noise voltages.

The improvement is obtained at the expense of response speed, so that several samples are now required before the balance point is (practically) reached. When the loop gain equals 0·2, the output is correct to within 1% in 21 samples, since

$$(1-A)^n = 0{\cdot}01$$

and

$$A = 0{\cdot}2.$$

Similarly, with a loop gain of 0·04, the output is correct to within 1% within 91 samples. Thus, for such high degrees of smoothing, a very high sampling density must be used. This facility is very useful when using a sampling scope in conjunction with a graph-plotter, where the scanning period can be sufficiently slow.

×10 AMPLIFIER AND OUTPUT CATHODE FOLLOWERS

The ×10 amplifier (Tr$_{34}$ in Fig. 13) uses an experimental transistor type in common-base configuration. The mean collector working point is 1mA and −25V. The amplified output is fed to an output cathode follower which serves to reduce the output impedance and prevent excessive loading from affecting the loop characteristics. Two output sockets are provided; one, which would be a front panel connection SKT$_7$, is intended for connection to the display scope; the other, SKT$_6$, would be at the rear of the instrument and permits simultaneous connection to a graph-plotter.

Part of the output is also applied to the feedback attenuator R$_{16}$ which adjusts the ratio between the output voltage at SKT$_6$ or SKT$_7$, and the input voltage to the probe, and hence the through-gain of the system. It also affects the loop gain, so that this control should be set up before finally adjusting the other loop controls.

Shift bias is introduced by R$_{14}$ and R$_{15}$, giving a maximum offset of about ±35V at the probe input. R$_{15}$ allows a vernier adjustment of ±1V.

The cathode follower V$_{4b}$ in Fig. 13 is used to lower the driving impedance to the feedback lines, one of which is capacitively loaded by the decoupling capacitor C$_{35}$ in the probe. The overall response time of the amplifier block from the grid of V$_3$ is less than 1μs. The resistor R$_{140}$ provides a collector supply voltage of about 1V for the probe amplifier transistor, Tr$_{25}$.

PERFORMANCE

A photograph of the complete attachment is shown in Fig. 14, and the performance of the unit is given under appropriate headings below.

Loop Characteristics

Waveforms 17 to 20 show the effects of various loop gains on a 2V pulse. In waveform 17, the adjustment is correct. Waveforms 18 and 19 show the effect of a high loop gain, and in waveform 20 the loop gain is reduced to about 0·25. (A similar effect is obtained by switching the 'RESPONSE' control to the ×5 smoothing position.)

Large-pulse Response

The response of the system to an 8V pulse, which is just less than the maximum input voltage, is shown in waveform 21, which shows that there is no appreciable lag or overshoot on either edge.

Rise-time and Overshoot

Waveform 23 shows the response of a typical sampling channel of the type described which has been in continuous service since mid-1962. The probes in this unit were made outside this laboratory, and do not have quite so fast a response as the prototype described in Ref.3. The time-scale here is 0·5ns/cm and gives an apparent rise-time of 0·85ns between the 10 and 90% points. Allowance must be made for the 0·43ns rise-time of the test-pulse, giving an actual value of 0·73ns, corresponding to a bandwidth of 480Mc/s. The input amplitude is 2·5V.

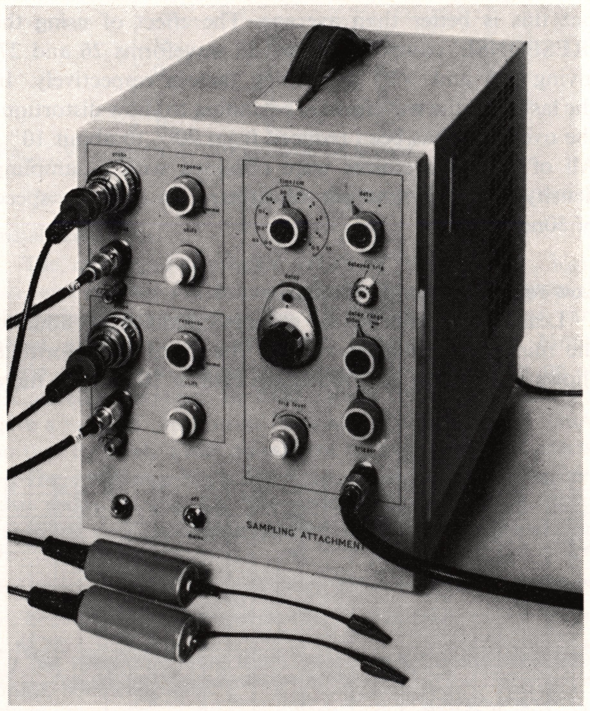

Fig. 14—Sampling attachment unit

The overshoot is seen to be about 3%, but much depends on the actual test conditions (the type of cables, terminations, etc.) and the figure can vary between 0% and 10%. It also increases slightly as the input amplitude is increased.

Pulse-response: Agreement between Channels

The responses of the two channels of the above oscilloscope are shown superimposed in waveform 24. It can be seen that there is good agreement between the two traces, both in response shape and time-balance. The 'TIME-BALANCE' control was adjusted three months before the waveform was made, which also illustrates the low time-drift between channels. The waveform also shows the small degree of jitter which can be obtained when the trigger circuits are correctly adjusted. The time scale is 0·2ns/cm.

Long-pulse Response

The response to a step input, continuing for at least 4μs, is shown in waveform 22. Very slight droop which can be noticed, is attributable to maladjustment of the capacitive attenuator.

Noise-level

The typical noise-level referred to the input of the attenuator is about 20mV peak. Waveform 25 shows a 100mV pulse, and indicates a noise level of about 10mV, but this is better than average. The effect of using the 'RESPONSE' control is shown in waveforms 26 and 27, giving ×5 and ×25 smoothing factors respectively. In the last case, the waveform is beginning to show distortion; the overshoot has been reduced from 20% to about 10%. All of these waveforms were obtained with a sampling density of 150 points per centimetre, at a sweep speed of 50ns/cm.

Low-repetition-rate Performance

Leakage currents in the storage circuit set a limit to the minimum repetition rate of the signal. Waveform 28 shows a 2V pulse at a repetition rate of 10c/s, and there is about 350mV of droop between samples. This is a constant figure, irrespective of pulse amplitude, so that the effect is more objectionable with small pulses. The droop can be greatly reduced by means of the 'RESPONSE' control; but a larger number of samples must be used, and this is inconvenient because of the long build-up time required.

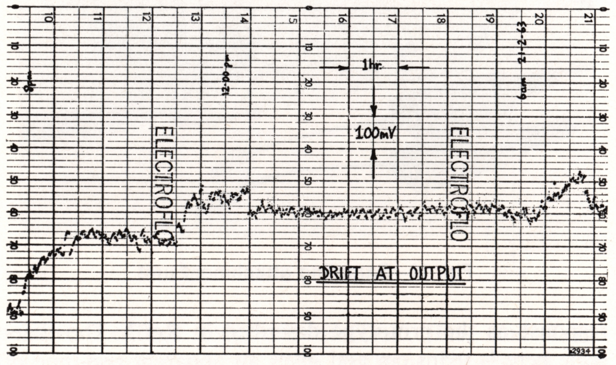

Fig. 15—Long-term drift at output

Drift

The drift over a twelve hour period is shown in Fig. 15. The highest drift rate noted was about 0·4V/hr. This is rather high, and was possibly caused through the use of d.c. offset voltages derived from the high voltage lines.

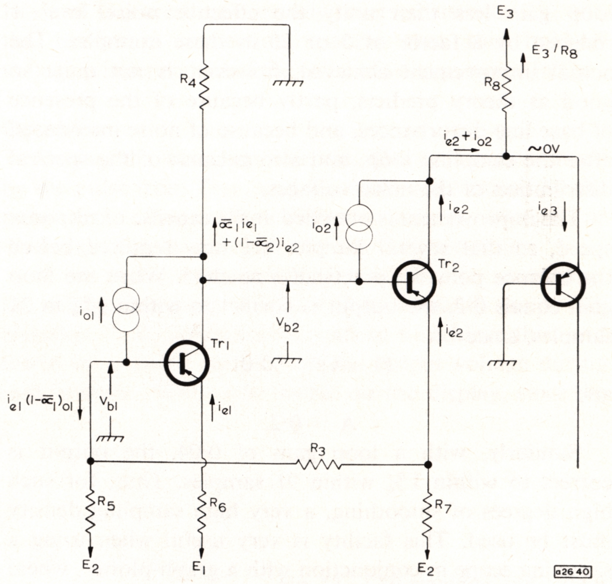

Fig. 16—D.C. circuit of pre-amplifier

```
                    STATISTICAL DESIGN OF CIRCUITS:
                    =DC FEEDBACK PAIR.

INPUT DATA:

 VARIABLE    NOMINAL   TOLERANCE   DISTRIBUTION   PARAMETER
    NO.       VALUE

     1     .1200/ 02        5.0          GAUSS   E1, VOLTS
     2     .2238/ 02        5.0          GAUSS   E2, VOLTS
     3     .4700/ 02        5.0           RECT   R3, KOHMS
     4     .1000/ 02        5.0           RECT   R4, KOHMS
     5     .1500/ 03        5.0           RECT   R5, KOHMS
     6     .3900/ 00        5.0           RECT   R6, KOHMS
     7     .6800/ 01        5.0           RECT   R7, KOHMS
     8     .6800/ 01        5.0           RECT   R8, KOHMS
     9     .9900/ 00        1.5          GAUSS   ALPHA BAR 1
    10     .9900/ 00        1.5          GAUSS   ALPHA BAR 2
    11     .2600/ 00       30.0          GAUSS   VBE1, VOLTS
    12     .3000/ 00       30.0          GAUSS   VBE2, VOLTS
    13    -.1400/ 02        5.0          GAUSS   E3, VOLTS
    14     .1500/-02  +900.0,-50.0       SKEW    101, MA

MEAN VALUES OF FUNCTIONS:

     F1= VB1= .1143/ 02
     F2= VB2= .7431/ 01
     F3= IE1= .7904/ 00
     F4= IE2= .2312/ 01
     F5= IE3= .2533/ 00

WORST CASE VALUES:

     F1(MIN)= .1067/ 02         ERROR=   -6.62  %
     F1(MAX)= .1215/ 02         ERROR=    6.36  %

     F2(MIN)= .6659/ 01         ERROR= -10.38  %
     F2(MAX)= .8826/ 01         ERROR=   18.78  %

     F3(MIN)= .5887/ 00         ERROR= -25.51  %
     F3(MAX)= .1095/ 01         ERROR=   38.51  %

     F4(MIN)= .1780/ 01         ERROR= -23.00  %
     F4(MAX)= .2776/ 01         ERROR=   20.05  %

     F5(MIN)=-.4952/ 00         ERROR=-295.51  %
     F5(MAX)= .9130/ 00         ERROR= 260.47  %

CIRCUIT ACCEPTED IF INSIDE THESE LIMITS:

     F1:               .1200/ 02   .1086/ 02
     F2:               .8174/ 01   .6688/ 01
     F3:               .8694/ 00   .7113/ 00
     F4:               .2543/ 01   .2081/ 01
     F5:               .5000/ 00   .0000/ 00

CONFIDENCE LEVELS:

     F1= 100.00  %
     F2=  98.90  %
     F3=  96.51  %
     F4=  98.01  %
     F5=  95.81  %

TOTAL NO. OF CIRCUITS MADE=   1003.
```

Fig. 17—Pre-amplifier analysis

COMPARISON OF SINGLE-SIDED SAMPLER WITH SYMMETRICAL SYSTEM

The following points of comparison can be made:

(1) *Balancing characteristics:* The single-sided system had unequal response to positive and negative changes, although compensation measures can be taken. In the symmetrical system, the loop gain tends to rise for changes of either sign. Also, when balanced, the symmetrical system produces negligible feedout of sampling pulses, whereas the single-sided system always produces some feedout.

(2) *Ease of Adjustment:* The initial adjustments tend to be difficult in both systems, if optimum operation is to be ensured. The symmetrical system tends to have more pre-set controls to set up, but it is easier to adjust loop gain characteristics, since there is no mean error signal, and no reference charge generator to adjust. In both systems, quite comprehensive test gear is required for setting up, and a mercury-switch pulse generator is indispensable.

(3) *Noise:* The symmetrical system is probably better when noise is considered, since noise on the sampling pulse (the main source) balances out in the gate. In the present case, the noise level at the sampling diode is about 2 to 4mV, compared to 1 to 2mV in typical symmetrical systems.

(4) *Bandwidth:* The symmetrical system can achieve high bandwidths, since the 'tips' of the sampling pulses can be used without the severe increase in noise level and overload effects which result when a single-sided gate is operated near the 'tip' of the sampling pulse.

(5) *Low-repetition Rate:* The symmetrical system is better here, since the store is being used to full capacity at all sensitivities, so that the droop between samples is a fixed percentage of this capacity at a given repetition rate. In the asymetrical system, the droop is a fixed voltage at a given rate, so is most noticeable on small signals.

(6) *Cost:* There is probably little difference in cost between the systems, but the single-sided system is inherently less complex, and the circuits described could probably be simplified further.

APPENDIX 1
D.C. Analysis of Pre-amplifier

The circuit considered is the well-known 'd.c. feedback pair', and is shown in Fig. 16. This analysis is to show that the pedestal current in Tr_{30} which occurs during the gating period, and the d.c. working points of the two transistors, are not so affected by component spreads as to require a pre-set control.

The circuit equations are

$$(1)\ V_{b(1)} = \left(i_{e(1)}(1\times\bar{\alpha}_1)-i_{o(1)}\right)\frac{R_3 . R_5}{R_3+R_5} + $$
$$+\ \frac{R_3}{R_3+R_5}(E_2-V_{b(2)}-V_{be(2)})+V_{be}+V_{be(2)}$$

$$(2)\ V_{b(2)} = R_4\left(\bar{\alpha}_1 i_{e(1)}+(1-\bar{\alpha}_2)I_{e(2)}-i_{o(1)}-i_{o(2)}\right)$$

$$(3)\ i_{e(1)} = (E_1-V_{b(1)}-V_{be(1)})/R_6$$

$$(4)\ i_{e(2)} = (E_2-V_{b(2)}-V_{be(2)})/R_7+$$
$$+(V_{b(1)}-V_{b(2)}-V_{be(2)})/R_3 .$$

It can be assumed that $i_{o(1)}$ and $i_{o(2)}$ are approximately equal and vary sympathetically with temperature. This gives

$$\begin{aligned}
K_1 . V_{b(1)} - R_5 . V_{b(2)} + K_2 . i_{e(1)} \qquad\qquad &= K_3\\
V_{b(2)} + K_4 . i_{e(1)} + K_5 . i_{e(2)} &= 0\\
V_{b(1)} \qquad + R_b . i_{e(1)} \qquad\qquad &= K_6\\
R_7 . V_{b(1)} - K_7 . V_{b(2)} \qquad + K_8 . i_{e(2)} &= K_9
\end{aligned}$$

$$\begin{aligned}
K_1 &= R_3+R_5\\
K_2 &= R_3R_5(1-\bar{\alpha}_1)\\
K_3 &= R_5V_{BE(2)}+R_eE_2-i_{o(1)}R_3R_5\\
K_4 &= -R_4\bar{\alpha}_1\\
K_5 &= R_4(1=\bar{\alpha}_2)\\
K_6 &= E_1-V_{BE(1)}\\
K_7 &= -(R_3+R_7)\\
K_8 &= -R_3R_7\\
K_9 &= (E_2\times V_{BE(2)})R_3-V_{BE(2)}R_7 .
\end{aligned}$$

Solving for $i_{e(2)}$ gives

$$i_{e(2)} = \left| \frac{\begin{matrix} K_1 & -R_5 & K_2 & K_3\\ 0 & 1 & K_4 & 0\\ 1 & 0 & R_6 & K_6\\ R_7 & K_7 & 0 & K_9 \end{matrix}}{\begin{matrix} K_1 & -R_5 & K_2 & 0\\ 0 & 1 & K_4 & K_5\\ 1 & 0 & R_6 & 0\\ R_7 & K_7 & 0 & K_8 \end{matrix}} \right|$$

$V_{B(1)}$, $V_{B(2)}$ and $i_{e(1)}$ can likewise be solved.

Then $i_{e(3)}=i_{e(2)}-\frac{E_3}{R_8}$, since the emitter of Tr_3 is at approximately zero volts.

The mean and worst-case values of $V_{B(1)}$, $V_{B(2)}$, $i_{e(1)}$, $i_{e(2)}$ and $i_{e(3)}$ for the given nominal values and tolerances of the variables are shown in Fig. 17. Notice that $i_{e(3)}$ can vary about ±250% of its mean value. However, using a Monte Carlo method, a statistical analysis was carried out on an Elliott 803 computer. In 1000 circuits 'built', less than 5% gave a value of $i_{e(3)}$ outside the limits of +0·00 to +0·50mA, so that R_8 rarely needs adjustment to correct pedestal effects.

The confidence levels for $V_{B(1)}$, $V_{B(2)}$, $i_{e(1)}$ and $i_{e(2)}$ are also shown in Fig. 17. The rejection limits were ±5% of mean for $V_{B(1)}$, and ±10% of mean for $V_{B(2)}$, $i_{e(1)}$ and $i_{e(2)}$.

APPENDIX 2
Notes on Waveforms

The waveforms were taken under the following conditions unless otherwise stated:

Oscilloscope:	Tektronix 545A with CA plug-in and ×10 P6000 probes or Type P6016 current probe.
Control settings:	Vertical shift to set output voltage to zero with input of probe earthed. Response control to '×1'. All other controls to give a stable display.
Trigger rate:	Varied, but normally about 25kc/s.

On the circuit diagrams, voltage and current waveforms are numbered where measurements were made.

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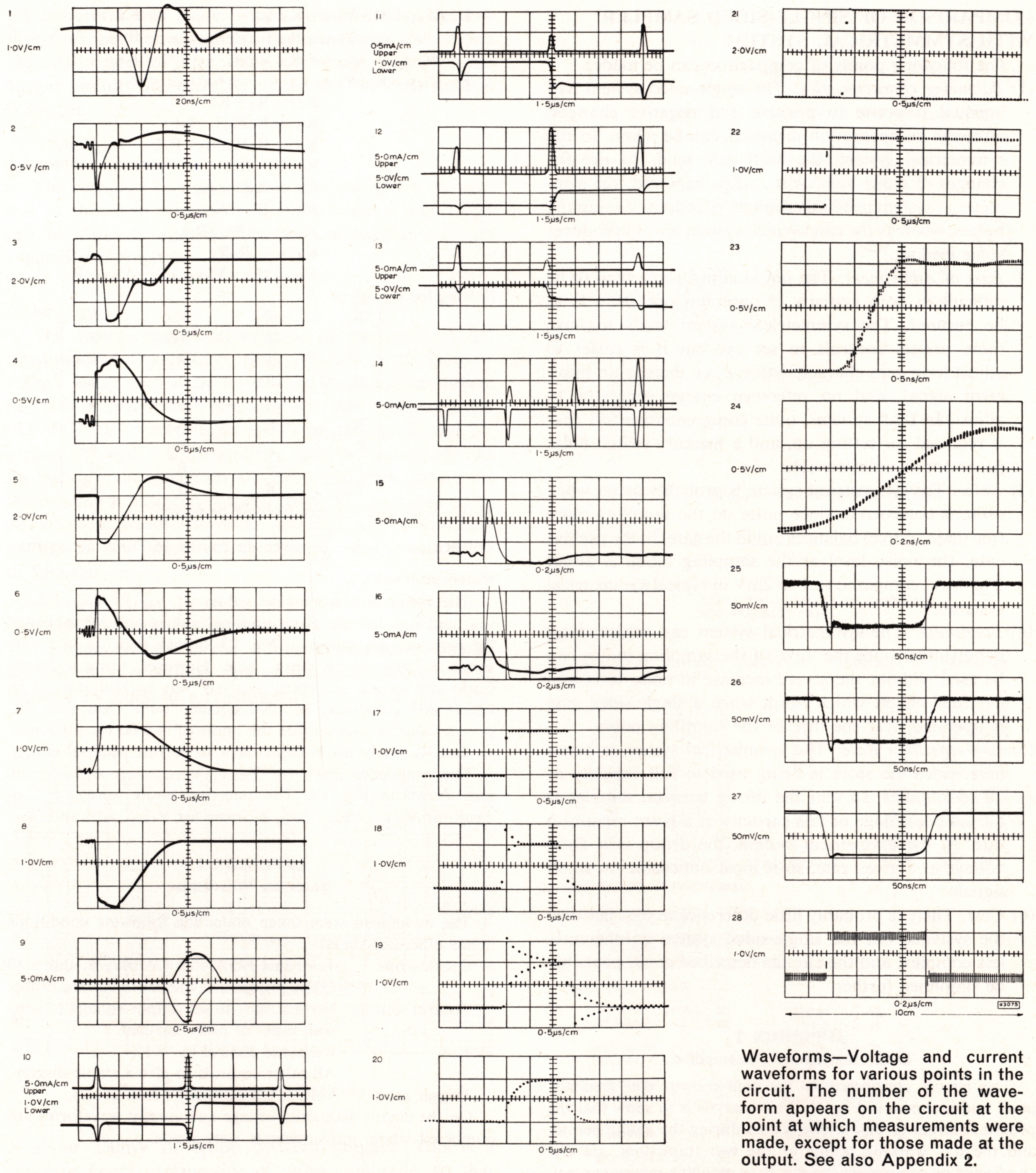

Waveforms—Voltage and current waveforms for various points in the circuit. The number of the waveform appears on the circuit at the point at which measurements were made, except for those made at the output. See also Appendix 2.

D.C. Inverters using ADZ11 and ADZ12 Transistors

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Push-pull inverters of the saturating drive transformer type (operating at 400c/s) and CR-timed type (operating at 2·5kc/s) have been designed round the Mullard ADZ11 and ADZ12 transistors. For both configurations, outputs of > 300W were obtained with the ADZ12 and a 28V supply, and > 120W with the ADZ11 and a 14V supply.

INTRODUCTION

Two d.c. inverter circuits have been designed round Mullard ADZ12 transistors for operation from a 28V supply. One of the circuits, of the two-transformer push-pull type (Refs.1 and 2), operates at 400c/s. The other, with CR timing (Ref.3), operates at 2·5kc/s. The maximum powers available from the circuits are about 325W and 300W respectively.

Variants of the two circuits, for use with ADZ11 transistors and a supply voltage of 14V, are also described. They provide maximum powers of about 125W.

Performance figures for the four inverters are given in Tables 1 and 2 on pages 306 and 307.

TWO-TRANSFORMER INVERTER

The two-transformer inverter is shown in Fig. 1. The circuit (Ref.2) consists of two transistors connected in push-pull, a linear output transformer T_2, and a saturating drive transformer T_1.

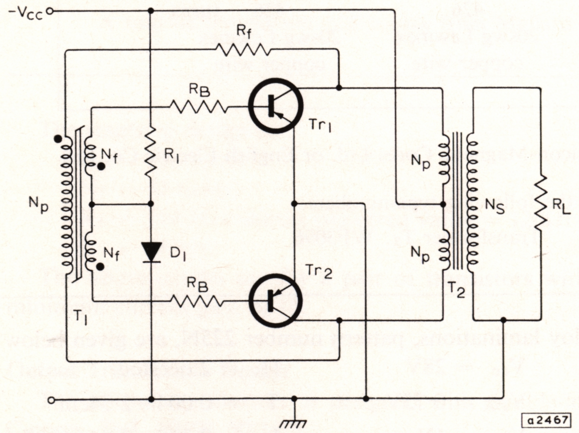

Fig. 1—Two-transformer inverter

The primary of the saturating transformer, in series with a feedback resistor R_f, is connected across the two collectors to control the operation. Series base resistors are used to reduce unbalance arising from spread in V_{be} of the transistors. In addition, R_1 and D_1 are used to ensure reliable starting on full load.

Design of Two-transformer Inverter

Several factors affect the design of a practical circuit. The transistor has a number of limitations which must be taken into account. First is the maximum collector voltage that can be applied, which in turn limits the maximum allowable supply voltage. Since ADZ12 transistors are rated at $V_{CEM} = -60V$, the maximum supply voltage is limited to 28V, allowing for a swing of 56V across the transistor which is cut off, and leaving sufficient safety margin for small fluctuations.

The second limitation is the maximum collector current that can be used. Although the ADZ12 is rated at $I_{CM} = 20A$, for d.c. inverter applications the peak collector current must be limited to 15A, as indicated in the transistor data under the permissible area of operation for the device.

The maximum power available from the push-pull pair is given by $P_{max} = \eta V_{cc} I_{CM}$, which is about 300W, allowing for the efficiency of the circuit, the voltage drop across the transistor, and the magnetising current of the transformer.

Drive Transformer Design

As indicated in Ref.2, the available voltage is equally divided between the voltage drop across the feedback resistor R_f and the voltage V_{in} developed across the primary of the saturating drive transformer T_1.

The equations listed below are used in the design of transformer T_1.

$$I_B = I_{CM}/\beta$$

$$V_f = V_{BE} + I_B . R_B + V_{D1}$$

$$n = V_{in}/V_f$$

$$I_{in} = I_B/n$$

$$R_f = \frac{2V_{cc} - V_{in}}{I_{in}} = \frac{V_{cc}}{I_{in}}, \text{ since } V_{in} = V_{cc}$$

$$N_p = \frac{H_s l_c}{1{\cdot}26 I_M}$$

$$N_f = N_p/n$$

$$f = \frac{V_{in} 10^8}{4 N_p A B_s}.$$

where A = TLS and T = lamination thickness, L = lamination width, S = number of laminations.

TABLE 1—Comparison of High-voltage and Low-voltage Inverters: Two-transformer Configuration

		High-voltage	Low-voltage	
Components				
Transistors		ADZ12	ADZ11	
Starting diode	D_1	BYZ13	BYZ13	
Starting resistor	R_1	820	680	Ω
Feedback resistor	R_f	120	33	Ω
Performance				
Supply voltage	V_{cc}	28	14	V
Supply current	I	13·4	12·5	A
Input power	P_{in}	375	175	W
Peak base current	I_{BM}	1·3	1·3	A
Peak collector current	I_{CM}	14·8	14·3	A
Output voltage	V_{out}	221	100	V
Load resistance	R_L	150	75	Ω
Output power	P_{out}	327	133	W
Efficiency	$\eta \times 100$	87	76	%
Frequency	f	408	416	c/s
Saturating Drive Transformer T_1				
Core		HCR alloy pattern 225N*	HCR alloy pattern 225N*	
No. of laminations		80	80	
Primary winding	N_p	136 27swg Lewmex copper wire	68 22swg Lewmex copper wire	turns
Secondary winding	N_f	33+33 bifilar 22swg Lewmex copper wire	33+33 bifilar 22swg Lewmex copper wire	turns
Linear Output Transformer T_2				
Core		Double-loop C-core type HWR 50/18/5†	Double-loop C-type type HWR 50/18/5†	
Primary winding	N_p	50+50 bifilar 15swg Lewmex copper wire	50+50 bifilar 15swg Lewmex copper wire	turns
Secondary winding	N_s	426 20swg Lewmex copper wire	426 20swg Lewmex copper wire	turns

*Telegraph Construction and Maintenance Co. Ltd. †Telcon-Magnetic Cores Ltd. or English Electric Co. Ltd.

Suitable transformers are available from Mullard Ltd. under the following type-numbers:

Transformer T_1: WF3095 Transformer T_2: WF3096

For efficient operation of the inverter, the magnetising current I_M should be a small fraction of the collector load current. Low magnetising current, however, calls for a high primary inductance, which in turn demands a large number of turns for all windings, for a given size of core. A compromise is therefore necessary, and the value of the magnetising current used is therefore adjusted on a practical basis.

The design values, with a square stack of Telcon HCR alloy laminations, pattern number 225N, are given below:

$V_{cc} = 28V$ $H_s = 2$ oersted
$V_{BE} = 0{\cdot}75V$ $T = 0{\cdot}004 \times 2{\cdot}54$cm
$V_{D1} = 1V$ $L = 0{\cdot}375 \times 2{\cdot}54$cm
$I_{CM} = 15A$ $S = 80$
$I_M = 100$mA $l_c = 8{\cdot}58$cm
$B_s = 15\,000$ gauss $R_B = 5\Omega$

where l_c is the length of the flux path.

TABLE 2—Comparison of High-voltage and Low-voltage Inverters: CR-timed Configuration

		High-voltage	Low-voltage	
Components				
Transistors		ADZ12	ADZ11	
Starting resistor	R_1	1000	470	Ω
Timing resistor	R_2	10	10	Ω
Timing capacitor	C	8	8	μF
Performance				
Supply voltage	V_{cc}	28	14	V
Supply current	I	13·5	12·5	A
Input power	P_{in}	378	175	W
Peak base current	I_{BM}	2·3	2·0	A
Peak collector current	I_{CM}	15	15	A
Output voltage	V_{out}	213	96·5	V
Load resistance	R_L	150	75	Ω
Output power	P_{out}	303	124	W
Efficiency	$\eta \times 100$	80	70·8	%
Frequency	f	2·5	2·3	kc/s
Linear Output Transformer				
Core		Single-loop C-core type HWR 50/24, in 0·002in strip*	Single-loop C-core type HWR 50/24, in 0·002in strip*	
Primary winding	N_p	32+32 bifilar 15swg Lewmex copper wire	32+32 bifilar 15swg Lewmex copper wire	turns
Feedback winding	N_f	22 20swg Lewmex copper wire	44 20swg Lewmex copper wire	turns
Secondary winding	N_s	273 19swg Lewmex copper wire	273 19swg Lewmex copper wire	turns

*Telcon-Magnetic Cores Ltd. or English Electric Co. Ltd.

A suitable transformer is available from Mullard Ltd. under the type-number WF3097.

The resulting design is:

$N_p = 136$ turns
$N_f = 33$ turns
$R_f = 116{\cdot}1\Omega$ (nearest preferred value $= 120\Omega$)
$f = 443$c/s.

The above results are for a pair of transistors with a minimum current gain of 15.

Output Transformer Design

The output transformer is designed with double-loop C-cores, Ref. HWR 50/18/5.

A compromise is again necessary, to keep the size of the transformer down. The magnetising current is therefore allowed to rise to 1·5A during each half cycle. This is satisfied by the following relation

$$L_p = V_p t_p / I_M$$

where $V_p = V_{cc} - V_c$ and $t_p = 1/2f$, therefore

$$L_p = \frac{(V_{cc} - V_c)10^3}{2f.I_M}$$

where L is in mH.

To ensure that the transformer is operating at a correct value of magnetising current, and at the same time has the required inductance, it is necessary to satisfy the following two equations for N_p.

$$N_p = \frac{10H(l_c + \mu l_g)}{4\pi I_M}$$

and

$$N_p = \frac{L_p\left(l_g + \frac{l_c}{\mu}\right)10^5}{4\pi A}$$

where

μ = permeability of the core material
l_c = length of flux path in cm
l_g = length of air gap in cm
L_p = inductance in mH.

The number of secondary turns is approximately given by

$$N_s = N_p(V_s/V_p)$$

and the maximum available power from the inverter is given by

$$P_{out} = \eta V_{cc} I_R$$

where $I_R = I_{CM} - I_M$.

The relevant design data are

$V_{cc} = 28V$ $\eta = 0{\cdot}8$
$V_c = 1V$ $f = 400c/s$
$V_s = 230V$ $A = 1{\cdot}032in^2$
$I_{CM} = 15A$ $l_c = 8{\cdot}12in$
$I_M = 1{\cdot}5A$ $l_g = 0{\cdot}00325in$

The resulting design is:

$H = 0{\cdot}495$ oersted
$P_{out} = 302{\cdot}4W$
$L_p = 22{\cdot}5mH$
$N_p = 50$ turns
$N_s = 426$ turns

Performance of the Inverter

A practical circuit was constructed on the basis of the above calculations. The measurements carried out on the circuit are given in Table 1 (page 306).

It is worth noting that a higher power is obtained than the value calculated. The discrepancy is due to the fact that for calculation purposes the efficiency was assumed to be 80%, whereas the measured efficiency is 87%. The calculations were repeated after substituting the measured value of efficiency of 87%, and the new calculated value of output power was found to be 328·9W.

Modification for 14V Supplies

The circuit was modified for use with 14V supplies and ADZ11 transistors, which have the same current rating as the ADZ12 but a lower voltage rating.

It was decided to use the same output transformer as for the 28V circuit, but to redesign the input transformer. The circuit specification and performance are given in Table 1.

It can be seen that the efficiency in this case is much lower. This is mainly due to the lower supply voltage, since the circuit losses are approximately the same.

INVERTER WITH CR TIMING

The inverter with CR timing is shown in Fig. 2. The main difference between this inverter and the two-transformer type is that the saturating transformer is replaced by a CR timing network. A linear output transformer is used as before, but a feedback winding is added to supply the required drive. Finally, the starting diode is replaced by two resistors R_2 which provide minimum forward voltage for reliable starting. These resistors, with the capacitor C, also control the timing of the inverter.

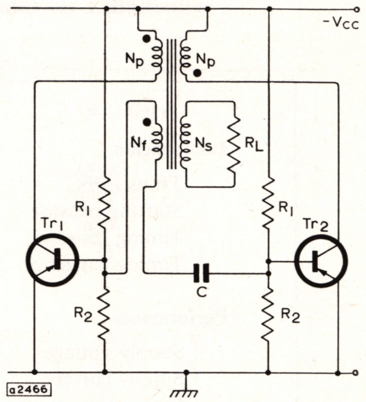

Fig. 2—Inverter with CR timing

Design of Inverter with CR Timing

Detailed design procedure of the inverter circuit with CR timing is given in Ref.3, so that it will not be repeated here. Only the necessary equations required for the design of a practical circuit are listed below.

The ADZ12 transistor is again used, therefore the comments on the voltage and current ratings apply to this design also.

Base Input Circuit and Timing Arrangement

The following equations are derived from the equivalent base input circuit (Ref.3).

$$I_{B(min)} = I_{CM}/\beta$$

$$I_{1(min)} = I_{B(min)} + \frac{I_{B(min)}R_o + V_o}{R_2}$$

$$V_f = \tfrac{1}{2}(I_{1(pk)} + I_{1(min)})\left(R_2 + \frac{R_2 . R_o}{R_2 + R_o}\right) + \frac{V_o . R_2}{R_2 + R_o}$$

(it is assumed that $I_{1(pk)} = 3I_{1(min)}$)

$$V_f = 2I_{1(min)}R_2\left(1 + \frac{R_o}{R_2 + R_o}\right)$$

$$C = \frac{10^6}{3{\cdot}2\, f\, R_2\left(1 + \frac{R_o}{R_2 + R_o}\right)}\,\mu F$$

$$R_1 = R_2(V_{cc}/V_T)$$

where V_T is the base-emitter voltage required to turn on the transistors sufficiently to ensure that the loop gain is above unity to start oscillation. For germanium power transistors, V_T is about 0·3V.

The above assumption of $I_{1(pk)} = 3I_{1(min)}$ is in accordance with the peak base current rating of the transistor, allowing for sufficient safety margin.

The following data were used for calculating the input circuit components.

$V_o = 0{\cdot}8V$ $I_{CM} = 15A$
$R_o = 1\Omega$ $\beta = 15$ and 30
$V_{cc} = 28V$ $f = 2{\cdot}5kc/s$
$V_T = 0{\cdot}3V$

The results were tabulated for various values of R_2, from which a set of values were selected corresponding to the nearest preferred values.

$R_2 = 10\Omega$
$R_1 = 1k\Omega$
$C = 8\mu F$
$V_f = 18{\cdot}4V$, which is the mean value required for the range of β specified above.

Output Transformer Design

The output transformer is designed with a single-loop C-core, Ref. HWR 50/24, in 0·002in strip.

Since the frequency of operation of the inverter is higher than in the two-transformer design, a lower value of inductance is required for limiting the magnetising current to a given value. Conversely, a lower magnetising current may be used with the same value of inductance. If the frequency of operation is high enough, as in this case, the primary inductance as well as the magnetising current may be reduced considerably, thus giving a smaller and lighter transformer.

The results were calculated for the following data,

$V_{cc} = 28V$ $\eta = 0{\cdot}8$
$V_c = 1V$ $f = 2{\cdot}5kc/s$
$V_s = 230V$ $A = 0{\cdot}69in^2$
$I_{CM} = 15A$ $l_c = 8{\cdot}12in$
$I_M = 1A$ $l_g = 0{\cdot}00325in$

and the resulting design was:

$H = 0{\cdot}46$ oersted $N_p = 32$ turns
$P_{out} = 313{\cdot}6W$ $N_f = 22$ turns
$L_p = 5{\cdot}4mH$ $N_s = 273$ turns.

Performance of the Inverter

A practical circuit was constructed on the basis of the above calculations. The circuit specification, and the performance with resistive load, are given in Table 2 (p.307).

Modification for 14V Supplies

The 28V inverter with CR timing was modified for use with 14V supplies and ADZ11 transistors. The two adjustments made were the doubling of the number of turns of the feedback winding, and the halving of the value of the starting resistor.

The specification and performance of the modified circuit are given in Table 2.

All measurements of the output voltage were made with a Dawe True-R.M.S. Valve Voltmeter Type 612A across the resistive load.

POWER AVAILABLE

The inverter circuits described in this article use linear output transformers. The peak collector current of the transistors is determined by the load current and the magnetising current of the transformer, and not by the available drive. Since, in the circuits described, the drive is always in excess of what is required for the maximum collector peak current, it is necessary to limit the load current so that the transistor ratings are not exceeded. With a resistive load the maximum power derived from the inverter should not exceed 140W for the 14V circuits and 330W for the 28V circuits.

With a reactive load the output power may need to be further limited so that the peak collector current of 15A is not exceeded.

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Transistor Coupling Circuits for the Z504S Stepping Tube

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This article describes a transistor pulse shaping circuit for coupling stepping tubes at speeds up to 400 p.p.s., and a 4000 p.p.s. blocking oscillator input circuit. In addition, two alternative light-sensitive input circuits are given, using ORP60 and RPY15 cadmium sulphide cells, for operation at counting speeds up to 25 p.p.s. and 13 p.p.s. respectively. The ORP60 operates satisfactorily with a drop in intensity of illumination from 2000 to 10 lux while the RYP15 requires 1000 lux falling to 10 lux. Auxiliary circuits for power supplies and resetting are also given.

INTRODUCTION

Two previous articles (Refs. 1 and 2) have described the operation of stepping tubes with valve and cold cathode trigger tube drive and coupling circuits. The present article gives a range of transistor drive and coupling circuits.

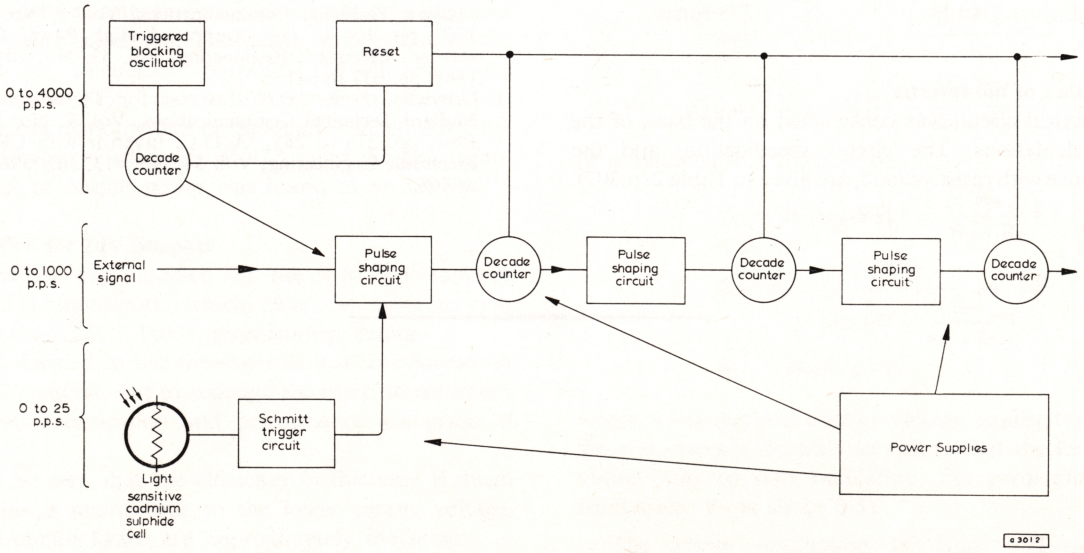


Fig. 1—Counter chain

The block diagram in Fig. 1 shows the arrangement of the circuits which are intended for operation at temperatures up to 50°C. The pulse shaper circuits are designed to produce pulses of defined shape and amplitude to drive the Z504S stepping tube. The basic pulse shaping circuit can be operated direct from an external signal at speeds up to 1000 p.p.s. Alternatively it can be driven from the k_9 output signal of a previous stepping tube at speeds up to 400 p.p.s.

Each pulse shaping stage uses an OC75 or ACY21 transistor followed by two ACY17 transistors in cascode. In principle, only two transistors are required for this circuit but a suitable high-voltage low-cost transistor is not available at present. By using a cascode circuit configuration two inexpensive ACY17 lower-voltage transistors can be used.

For operation at the maximum recommended speed of 4000 p.p.s. a triggered blocking oscillator circuit is given. The blocking oscillator design is used since it gives a pulse magnitude which can be closely controlled, and is substantially independent of environmental variations.

A light-sensitive input circuit using cadmium sulphide cells is also given for applications such as production line counting from 0 to 25c/s. This circuit has the advantage that it can sense object size or colour. It can therefore be used in applications where mechanical contacts are impracticable.

This article includes details of a resetting circuit to enable the Z504S scaler to be reset to zero. A power supply unit that provides the required voltages in an economical manner is also given.

Pulse Shaping Circuit

The basic pulse shaping circuit for coupling the output of one stepping tube to the input terminals of the next tube is given in Fig. 2, and the operating waveforms are shown in Fig. 3. It consists of a single transistor current amplifier Tr_1 followed by a pair of transistors connected as a cascode circuit designed to drive the guide A cathodes of the succeeding stepping tube. The guide B waveform is derived from the guide A circuit through an integrator network.

Since the stepping action in the second stage is actuated by the discharge leaving the k_9 cathode in the previous stepping tube, there is only a short delay in stepping a chain of tubes from, for example, 0999 to 1000. This circuit system may therefore be more attractive for batching and timing applications than valve and cold cathode tube circuits (Refs. 1 and 2), where considerable delays occur in the 'carry' down the chain.

CIRCUIT OPERATION

When the discharge is on cathodes 0 to 8 of tube V_1, the resistor R_2 defines the base current of transistor Tr_1. The value of R_2 is chosen so that $I_b > I_c/h_{fe}$, and Tr_1 is therefore bottomed. In a similar manner resistors R_4 and R_5 are chosen so that transistors Tr_2 and Tr_3 are also bottomed. Under these conditions the collector of Tr_3, and hence the guide A cathodes of the succeeding stepping tube, closely approach the positive supply voltage $+V$

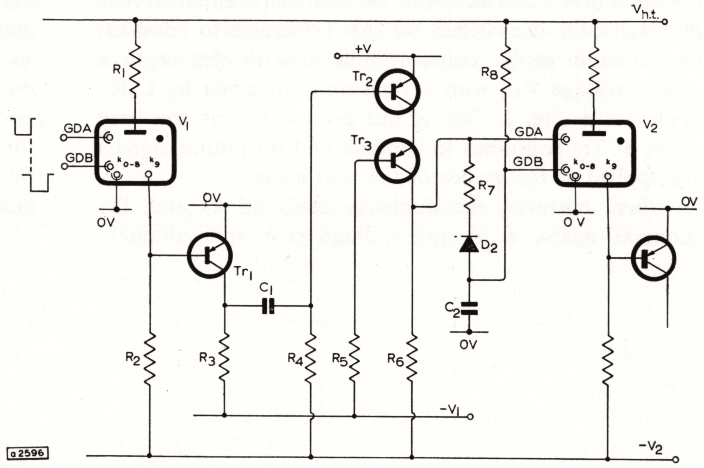


Fig. 2—Basic pulse shaping circuit

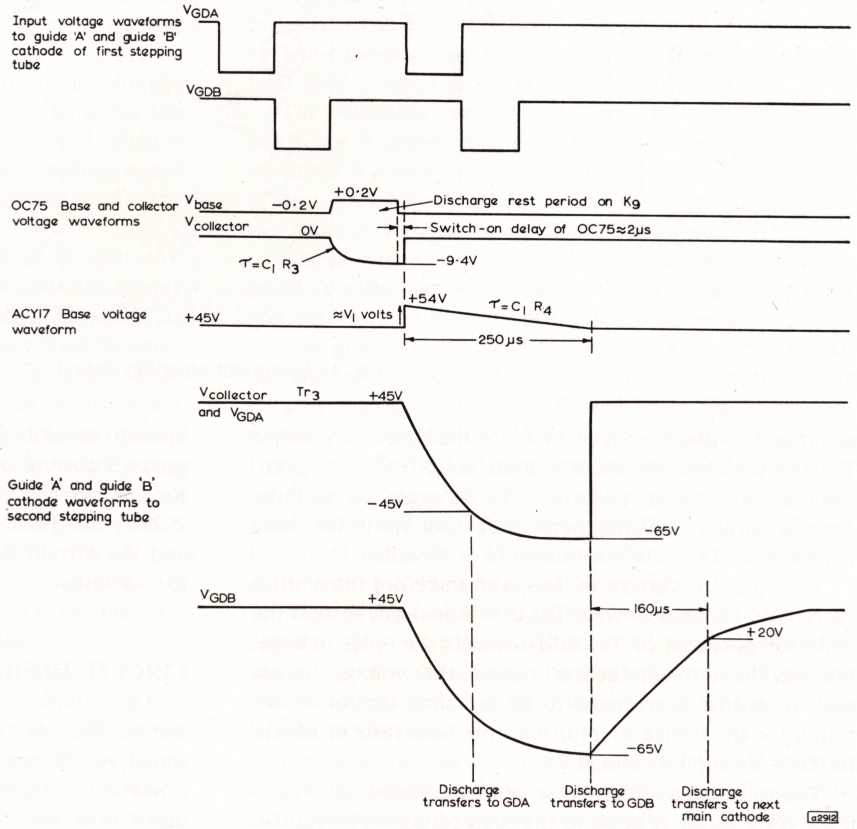


Fig. 3—Pulse shaper waveforms

volts. The guide B cathodes will also be at approximately +V volts because of the current flowing through R_8, D_2 and R_7. This supply voltage constitutes the positive guide bias of the stepping tube V_2.

When the discharge steps on to k_9 in the first stage, the flow of cathode current through R_2 causes the base potential of Tr_1 to rise above the emitter potential so that this transistor is switched off. As Tr_1 ceases to conduct, the potential of the collector falls towards the negative supply voltage V_1, with a time-constant given by C_1R_3 as shown in Fig. 3. During this process the emitter-base diode of Tr_2 continues to conduct and no output signals are applied to the guides of the next stage.

When, however, the discharge steps off k_9 and Tr_1 conducts again, a positive voltage step approximately equal to V_1 volts is applied by C_1 to the base of transistor Tr_2 and the cascode circuit is switched off. C_1 then commences to discharge towards $-V_2$ through R_4, and the cascode circuit remains non-conducting until the base potential of Tr_2 falls once more to +V volts.

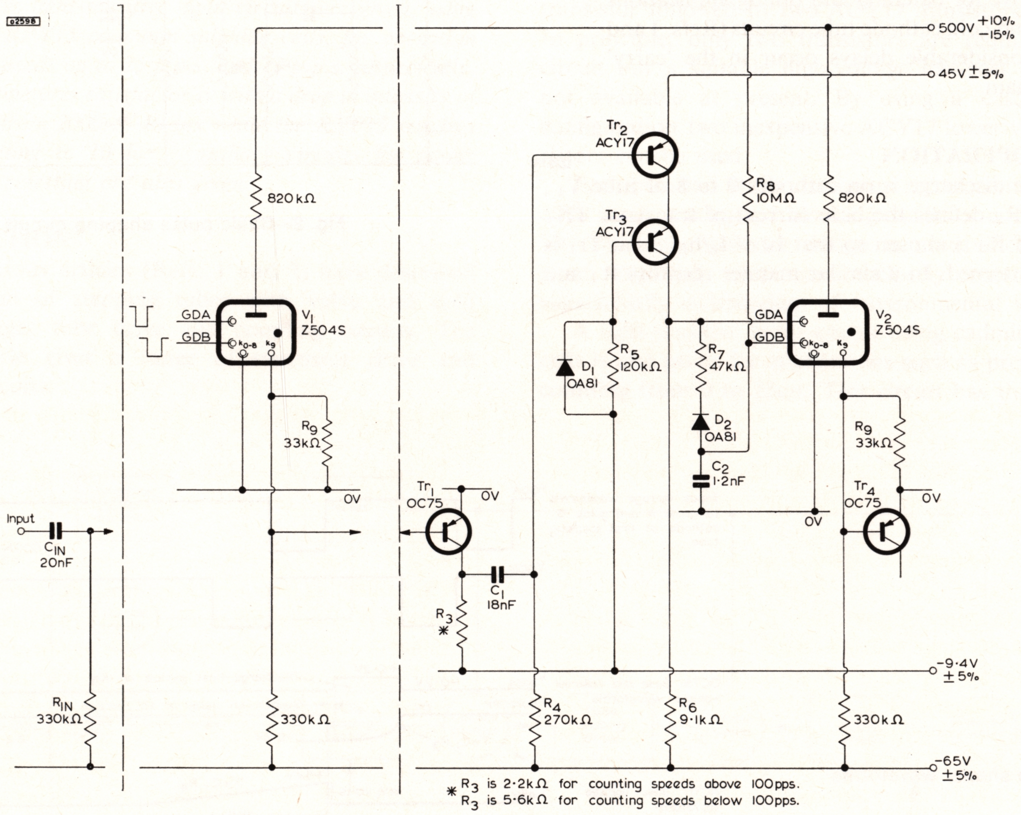


Fig. 4—Complete coupling circuit

The collector current of Tr_2, and therefore the emitter current of Tr_3, cease when Tr_2 is switched off, so that the collector potential of Tr_3 falls towards the $-V_2$ voltage. During the non-conduction period the voltage across each transistor is arranged to be less than the maximum rating for the device by returning the base resistor of Tr_3 to the $-V_1$ supply voltage.

The negative voltage pulse at the collector of Tr_3 is used as the guide A pulse to the succeeding stepping tube. The duration of the pulse is determined by the time-constant C_1R_4, together with the supply voltages V_1 and V_2. The guide B pulse is derived by means of the integrator circuit consisting of R_6, R_7 and C_2.

As the guide A potential falls, C_2 commences to discharge through R_7 and R_6. The time-constant $C_2(R_6$ and $R_7)$ is designed to permit the potential of the guide B cathodes to fall to substantially the same level as the guide A cathodes before the end of the guide A pulse period. Thus, when transistors Tr_2 and Tr_3 conduct once more and the guide A pulse ends, the potential of the guide B cathodes is held instantaneously at $-V_2$ volts by capacitor C_2 so that the discharge transfers to the guide B cathode adjacent to the glowing guide A cathode.

The potential at the guide B cathodes then rises nearly linearly towards $V_{h.t.}$ as capacitor C_2 is charged by the guide B current and the current flowing through resistor R_8. When the guide B cathodes reach approximately +20V, the discharge transfers to the next main cathode and the current through R_8 completes the recharge of C_2 to +V volts.

CIRCUIT DESIGN

The complete circuit of one pulse shaper is shown in Fig. 4. This may be driven either direct from an external signal via the network $C_{IN}R_{IN}$ or from the k_9 cathode of a previous stepping tube V_1. The input requirements for direct operation are given later under *External Drive to the Pulse Shaper* (page 314) and the design is now described simply as a coupling circuit.

Choice of Anode and Guide Circuit Supply Voltages

To keep power supply costs to a minimum, an unstabilised h.t. supply is used for the stepping tube and the anode resistor is chosen to accommodate supply voltage variations of +10% and −15%. Also the nominal tube current is kept as low as possible, within the 250 to 525μA permitted current range, to give maximum tube life. With the selected h.t. value of 500V +10% to −15%, the anode load resistor of 820kΩ ±7%, and a maintaining voltage range of 183 to 198V, a current operating range of 260 to 480μA is obtained.

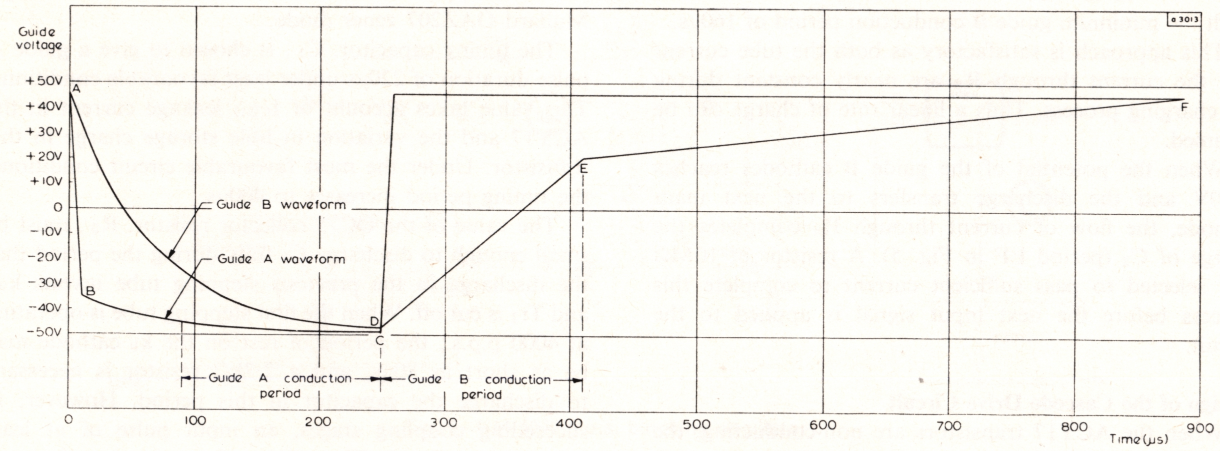


Fig. 5—Guide A and B waveforms during stepping

The Z504S requires a positive guide supply voltage of 45V for reliable operation at 4000 p.p.s. To avoid the use of separate guide supply lines in the circuit when a 4000 p.p.s. input stage is used, both the coupling stages and the first tube in the scaler are operated with a common guide supply voltage of 45V.

In addition, a negative guide voltage of at least 45V is required to ensure reliable stepping. A collector supply voltage greater than this value is necessary, however, as a voltage drop occurs across the collector load resistor, R_6, during the guide A conduction period. The voltage drop across R_6 is determined by the sum of the transistor leakage currents in the cascode circuit, the maximum guide A current and the charging current of the integrator capacitor C_2. To minimise the transistor current during conduction, a collector load resistor of 9·1kΩ was chosen together with a collector voltage of −65V. This is the optimum combination which avoids the use of transistors with a higher voltage rating. The operation of this part of the circuit is detailed in the next section.

Guide Circuit Design

Fig. 5 shows the waveform requirements at the guide A and B cathodes during stepping. When Tr_2 and Tr_3 are switched off, the potential of the guide A cathodes follows the curve ABC. The exponential fall of voltage (from B to C) is determined by the discharge of C_2 via R_7 and R_6. The ultimate level to which the guides A fall is defined by the voltage drop across R_6. This voltage drop is determined by the sum of the ACY17 leakage currents and the guide A current. A maximum I_{CBO} leakage current of 250μA at 50°C is assumed for each ACY17, and under these conditions an ultimate negative guide A voltage of at least −52V is available in the circuit. This leakage current figure is considerably greater than the expected worst life value, so that a long life reliability may be expected.

The guide B waveform is shown as the curve ADEF in Fig. 5. The exponential fall in voltage (AD) is defined by the time-constant C_2 (R_7 and R_6) seconds, and the final level is equal to the guide A potential.

The following requirements must be satisfied during the guide A conduction period. First, it is necessary for the guide A potential to become more negative than −45V, at least 60μs before the guide A pulse is terminated. Also the guide B voltage should remain at some 20V positive compared with that of the guide A cathodes, until the guide A cathodes reach −45V. Thus the discharge does not step back to the previous guide B cathode.

The guide B voltage must be at least −45V before the end of the guide A pulse period. This requirement ensures a guide A to guide B step when the transistors switch into conduction once more. The circuit shown in Fig. 4 satisfies these requirements under all operating conditions. When the cascode circuit is switched off for a period of at least 220μs, the guide A potential falls, in the worst case, to −45V after 130μs. Thus a guide A pulse period $\geqslant$ 90μs is always available.

When the cascode transistors are switched into conduction again, the guide A potential rises rapidly and diode D_2 is reverse biased. The guide B conduction period (DE in Fig. 5) is then defined by the recharge time of the integrator capacitor, C_2.

For maximum circuit reliability, it is desirable to have a long discharge rest period on the guide B cathode during stepping. In this design the value of the integrator capacitor is chosen to give a guide B conduction period of 160µs under least favourable conditions. The conduction period is defined from the end of the guide A pulse until the potential of the guide B cathodes has risen to some +20V above main cathode potential.

The value of C_2 is calculated from the equation

$$C_2 = (I_{GDB}+I_{R8})\frac{dt}{dV},$$

where

dV = voltage excursion of the guide B cathodes −52 to +20V

dt = minimum guide B conduction period of 160µs.

This approach is satisfactory as both the tube current and the current through R_8 are nearly constant during the charging process. Thus a linear rate of charge can be assumed.

When the potential of the guide B cathodes reaches +20V and the discharge transfers to the next main cathode, the flow of current through R_8 completes the charge of C_2 (period EF in Fig. 5). A resistor of 10MΩ was selected to pass sufficient current to complete this process before the next input signal is applied to the circuit.

Design of the Cascode Drive Circuit

When the ACY17 transistors are non-conducting, the base potential of Tr_3 (and hence its emitter potential) must be such that there is less than 60V developed across the collector-emitter junction of each ACY17. In addition a positive voltage pulse is present at the base of Tr_2 during the non-conduction period, and the collector-base breakdown voltage difference must not exceed 70V. These conditions are satisfied by returning the base resistor of Tr_3 to a potential between −3 and −13V. For convenience the resistor is returned to the 9·4V negative supply used to drive Tr_1.

The base resistor of Tr_2 is returned to the −65V line and acts as a semi-constant current generator to discharge capacitor C_1 during the cascode circuit non-conduction period. With this approach, large changes in the timing period, due to variations in supply voltages and I_{CBO} leakage current, are avoided.

An OA81 diode is connected across the Tr_3 base resistor to overcome a hole storage effect in the cascode circuit. When the cascode circuit is suddenly switched off, the base current in each transistor reverses and a considerable reverse current can flow until the stored holes are neutralised. In the absence of the diode the base potential falls considerably below the −9·4V reference level, resulting in the V_{CB} rating of the upper ACY17 being exceeded. The diode, however, clamps the base at −9·4V and, in addition, offers a low impedance path to the base reverse current so that the hole storage delay is reduced to a minimum.

First Transistor Amplifier

When the discharge in the previous stepping tube leaves k_9, Tr_1 conducts and the positive voltage step at the collector of the transistor is applied via C_1 to the base of Tr_2. To avoid exceeding the V_{BE} voltage limit for an ACY17 transistor, Tr_1 is operated from a −9·4V nominal supply which can be obtained from a single Mullard OAZ207 zener diode.

The timing capacitor, C_1, is chosen to give a guide A pulse duration of 220µs under least favourable conditions. This value takes account of I_{CBO} leakage current in the ACY17 and the variation in hole storage charge in this transistor. Under the most favourable circuit conditions, the timing period increases to 400µs.

The value of the OC75 collector resistor, R_3, must be small enough to discharge C_1 fully during the period that the discharge in the previous stepping tube invests k_9, and Tr_1 is cut off. When the first stepping tube is operating at 4000 p.p.s., the period of rest on the k_9 cathode may be as short as 80µs, and a 2·2kΩ resistor is necessary to discharge the capacitor in this period. However, in succeeding coupling stages, an input pulse of at least 2·5ms is available. Thus the resistor in the 40 p.p.s. stage and below may be increased to 5·6kΩ with a corresponding reduction in collector current.

A current gain, h_{fe}, of at least 35 has been assumed throughout the life of the OC75. With this current gain, a base current of 180µA is necessary to bottom the OC75, under the worst operating conditions. When this base current is obtained with a resistor of 330kΩ, which is returned to the −65V line, the minimum expected discharge current at the k_9 cathode is sufficient to ensure that the OC75 is cut off.

A 33kΩ resistor is connected between the base and the emitter of the OC75. This resistor limits the positive voltage at the base to less than 10V when the k_9 cathode current rises to a maximum value of 480µA.

External Drive to the Pulse Shaper

Where operation at input counting speeds of ⩽ 1000 p.p.s. are required, the base of the OC75 may be driven from an external signal as shown in Fig. 4. A positive pulse of at least 2V amplitude having a minimum duration of 80µs must be applied to the input capacitor C_{IN}. The maximum input pulse amplitude must be limited to 10V, to avoid exceeding the reverse voltage rating of the OC75 emitter-base junction.

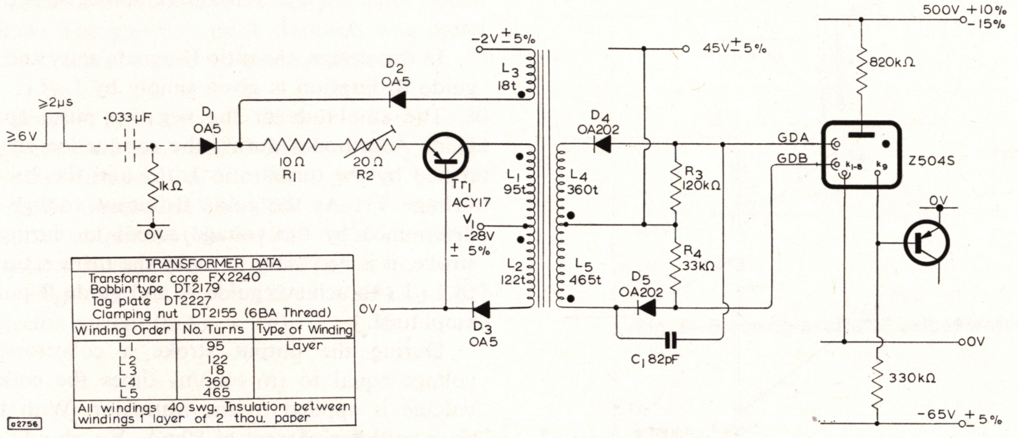
4000 p.p.s. Input Drive Circuit

When it is desired to count input signals at speeds greater than 1000 p.p.s., a further pulse shaping circuit is required. For maximum reliability it is desirable to obtain a close control of guide pulse shape and amplitude. A triggered blocking oscillator was selected for this application as the output pulses can be made substantially independent of variations caused by temperature or the effects of surrounding circuitry.

TRIGGERED BLOCKING OSCILLATOR

A 4000 p.p.s. blocking oscillator for driving the first Z504S in a counter chain is shown in Fig. 6. A single ACY17 transistor drives a transformer which generates a 70µs guide A pulse, followed immediately by a 95µs guide B pulse. The circuit is triggered by a positive signal at the input terminal.

The durations of the guide A and B pulses are defined by the collector primary and clamp windings L_1 and L_2, and the emitter current during the conduction stroke. The voltage across the emitter winding L_3 and the current limiting resistors R_1 and R_2 determine the emitter current during conduction. The variable resistor R_2 enables the oscillator conduction period to be set precisely at 70µs.



TRANSFORMER DATA		
Transformer core FX2240 Bobbin type DT2179 Tag plate DT2227 Clamping nut DT2155 (6BA Thread)		
Winding Order	No. Turns	Type of Winding
L1	95	Layer
L2	122	
L3	18	
L4	360	
L5	465	
All windings 40 swg. Insulation between windings 1 layer of 2 thou. paper		

Fig. 6—0 to 4000 p.p.s. blocking oscillator

The output waveforms are applied direct to the guide A and guide B cathodes of the stepping tube. Diodes D_4 and D_5 disconnect the guide cathodes from the windings L_4 and L_5 during the positive voltage stroke of each winding so that only the negative portions of the output pulses are applied to the guide cathodes of the stepping tube.

The voltage and current waveforms which occur in the circuit are given in Fig. 7. When a positive pulse is applied to the input diode, D_1, the emitter potential of Tr_1 is raised above base potential, and the transistor starts to conduct. A back e.m.f. is then generated across winding L_1, the collector potential of the transistor rises from −28V and the transistor bottoms at approximately zero volts. The voltage developed across the feedback winding L_3 is applied via diode D_2 to the emitter circuit to maintain the conduction process.

The duration of the conduction period is determined by the linear increase of collector current in the primary winding L_1. When this current reaches a value equal to $h_{fb}.I_e$ (where I_e is the emitter current) the increase in collector current ceases and the voltages across the transformer windings start to collapse. The energy stored in the transformer core then causes a rapid reversal of the transformer voltages until the voltage developed across the clamp winding L_2 exceeds 28V and diode D_3 conducts. Current then flows from the −28V supply through winding L_2 and the clamp diode until the energy in the core approaches zero, when the transformer winding voltages fall to zero once more. The rapid reversal of voltage at the feedback winding also serves to switch the transistor into non-conduction at the end of the forward stroke.

The advantage of using an additional winding, L_2, for clamping during the output stroke of operation is that a reversal of current occurs in the collector supply and the maximum mean collector supply current is reduced from 12mA to approximately 8mA.

Design Considerations

The circuit diagram of the complete blocking oscillator together with the transformer data is shown in Fig. 6.

The duration of the conduction or guide A period is given by the equation

$$\tau_{conduction} = \tau_{GDA} = \frac{L_1(h_{fe}.I_e - I_{load})}{V_1} \text{ seconds}$$

where

L_1 = inductance of the collector winding

V_1 = collector supply voltage

I_{load} = current reflected into the collector winding L_1 due to emitter current in winding L_3.

The emitter current I_e is defined as

$$I_e = \frac{V_{L3} - V_{D2} - V_{be} - 2}{R_1 + R_2} \text{A}$$

where

V_{L3} = voltage generated across the feedback winding L_3

V_{D2} = forward voltage drop across diode D_2.

To ensure stability in the conduction period, a stable collector supply voltage is required and the emitter current must remain constant. Variations in emitter current due to changes in temperature are minimised by making the feedback voltage, V_{L3}, large compared with the voltage variations expected in diode D_2 and the base-emitter junction of the transistor. Emitter current changes have

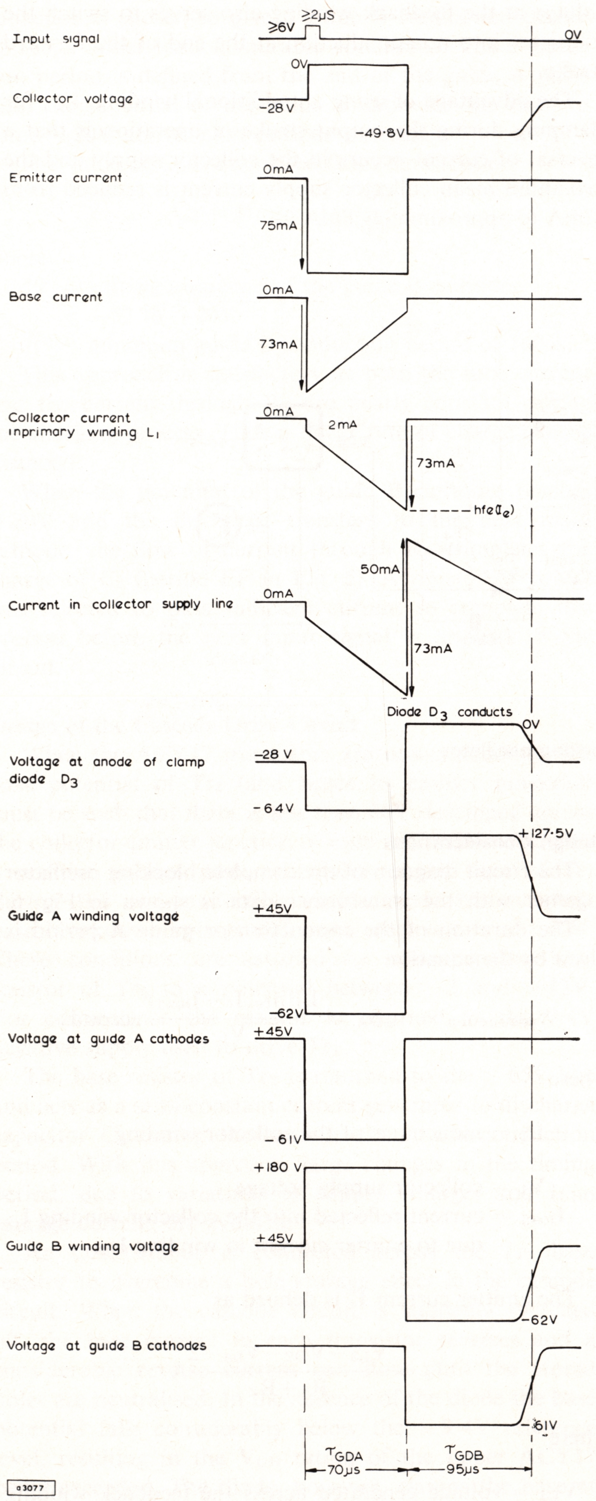


Fig. 7—Blocking oscillator voltage and current waveforms

been further reduced by using a gold-bonded diode with a low forward voltage drop.

When the circuit switches from the conduction stroke to the output or guide B stroke of operation, both the duration and amplitude of the guide B output pulse are defined by the voltage developed across clamp winding L_2.

The ratio of the output stroke period τ_{GDB} to the conduction stroke period τ_{GDA} is given by the equation

$$\frac{\tau_{GDB}}{\tau_{GDA}} = K\frac{L_2}{L_1}$$

where

$$K = \left(\frac{\text{the voltage developed across } L_1 \text{ during the conduction stroke}}{\text{the voltage developed across } L_2 \text{ during the output stroke}}\right)$$

In this design, the ratio K equals unity and the required guide B duration is given simply by L_2/L_1.

The amplitude of the negative pulse applied to the guide A cathodes during the conduction stroke is determined by the turns ratio L_4/L_1 and the collector supply voltage V_1. As the guide B output voltage is, however, determined by the voltage across L_2 during the output stroke, it is necessary to make the turns ratio L_5/L_2 equal to L_4/L_1 to achieve guide A and guide B pulses of equal amplitude.

During the output stroke a collector-base reverse voltage equal to $(n_1+n_2)/n_2$ times the collector supply voltage is applied to the transistor. With the designed peak collector current of 80mA, V_{cb} should be restricted to $\leqslant$ 58V, so that the maximum permitted collector supply voltage is therefore $V_{cb}.n_2/(n_1+n_2) = 33$V. For convenience the collector circuit is designed to operate from a chain of three OAZ207 zener diodes, giving a negative supply voltage in the range 26·4 to 30V.

Output Circuit

Resistors R_3 and R_4 in the guide cathode circuit return the guides to the positive supply voltage when no input signal is received. R_3 is made as large as possible to reduce the load effect on the transformer during the guide A stroke. The guide B resistor, R_4, however, also serves to dissipate the remaining energy stored in the core at the end of the guide B stroke. The value of R_4 must be low enough to limit the voltage overswing in the transformer windings so that the voltage developed across the feedback winding cannot switch the circuit into conduction again at the end of the guide B stroke.

In this circuit a gap of approximately 10µs occurs between the guide pulses at the transformer output terminals. The gap is avoided at the guide cathodes, however, by inserting capacitor C_1 between the guide A cathode and the guide B transformer winding, so that the guide A potential is held negative for the duration of the 10µs switch-over period. The guide A potential thus returns to the positive guide voltage level only after the guide B pulse has reached full amplitude. The dotted line in Fig. 8 indicates the end of the guide pulse at the transformer, and the solid line the pulse at the guide A cathodes.

Input Drive Requirements

The blocking oscillator is triggered when a positive pulse $\geqslant$ 6V in amplitude and $\geqslant$ 2µs duration is applied to the anode of diode D_1. The input current under these conditions is approximately 80mA. It is more convenient, however, to apply the input signal to the resistor-capacitor network shown dotted in Fig. 6, where the input pulse is differentiated during the conduction period. With this arrangement there is no necessity to restrict the trigger pulse duration to less than the period of conduction in the blocking oscillator. Under these conditions the minimum trigger pulse requirements are still 6V and 2µs and the maximum permitted pulse amplitude is 20V.

Performance

The performance of a typical blocking oscillator circuit is given below. The guide A pulse duration was preset to 70µs under nominal supply voltage conditions.

		Nominal	
Supply voltage (V)	26·4	28·2	30
Guide A pulse duration (µs)	66	70	72
Guide B pulse duration (µs)	92	95	100
Guide A pulse amplitude (V)	−107	−115	−120
Guide B pulse amplitude (V)	−100	−107	−113
ACY17 collector-base			
Reverse voltage (V)	−52	−54	−57
Peak collector current (mA)	70	75	80

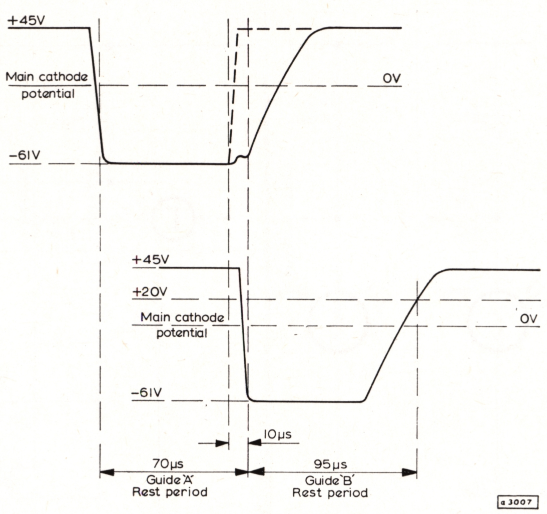


Fig. 8—Blocking oscillator output waveforms

Light-sensitive Input Circuit

It is often required to count a series of articles on a production line or in similar applications where mechanical contacts are an embarrassment or where object size or colour is of importance.

The cadmium sulphide cell was selected for this application because of its large, although relatively slow, response to changes in illumination and its freedom from thermal effects at temperatures up to at least 60°C. The slow response of the cell is not a serious disadvantage as the majority of production line counting applications have speed requirements well below the maximum operating speed of a cadmium sulphide cell.

The circuit diagram of a light-sensitive input stage is given in Fig. 9. Two alternative cadmium sulphide input designs are given, one cell requiring a greater intensity of illumination than the other. The output from the cells is fed to a Schmitt trigger circuit. The Schmitt trigger circuit is incorporated into the design to generate a pulse of defined rise time to operate the ACY17 cascode circuit.

CIRCUIT OPERATION

To consider the operation of the circuit, assume that the cadmium sulphide cell is illuminated, its resistance is low, and Tr_1 is therefore conducting and bottomed. Transistor Tr_2 is now held non-conducting because its emitter is returned to the common emitter resistor R_6 at a potential of approximately −2V and the base is returned to approximately −1V by the potential divider R_5, R_7 and R_8. Under these conditions the collector of Tr_2 rests at −9·4V and both ACY17 cascode transistors are bottomed.

When the illumination is removed, the resistance of the cadmium sulphide cell increases and the base potential of Tr_1 rises so that the transistor starts to come out of the bottomed condition. The base of Tr_2 becomes more negative as the collector potential of Tr_1 falls, and at the same time the emitter potential of both transistors rises toward zero volts. At the instant Tr_2 starts to conduct the circuit switches suddenly to the condition where Tr_1 is cut off and Tr_2 is conducting heavily and is bottomed.

At this instant, a positive pulse of approximately 6·6V is applied via capacitor C_1 to the base of the cascode transistor Tr_3 and the cascode circuit is switched into non-conduction. Capacitor C_1 then discharges through the base resistor R_{10} until after approximately 250µs the base of Tr_3 again becomes more negative than the emitter and the cascode transistors are switched back into conduction.

The application of the positive pulse to the ACY17 circuit causes the coupling circuit to operate and the discharge in the stepping tube is transferred to the next main cathode as described on page 311.

When the illumination is re-applied, the base voltage of Tr_1 falls again and Tr_2 starts to conduct. The circuit then switches back rapidly to the original stable state with Tr_1 conducting and Tr_2 cut off. The collector potential of Tr_2 falls exponentially to −9·4V as C_1 discharges through R_9.

The circuit therefore counts only when the cell illumination is obscured, and not when the illumination is re-applied to the cell, so that only one input pulse is applied to the counter for each object that is sensed.

PERFORMANCE

Table 1 shows the performance of the ORP60 and the RPY15 cadmium sulphide cells driving the Schmitt trigger circuit.

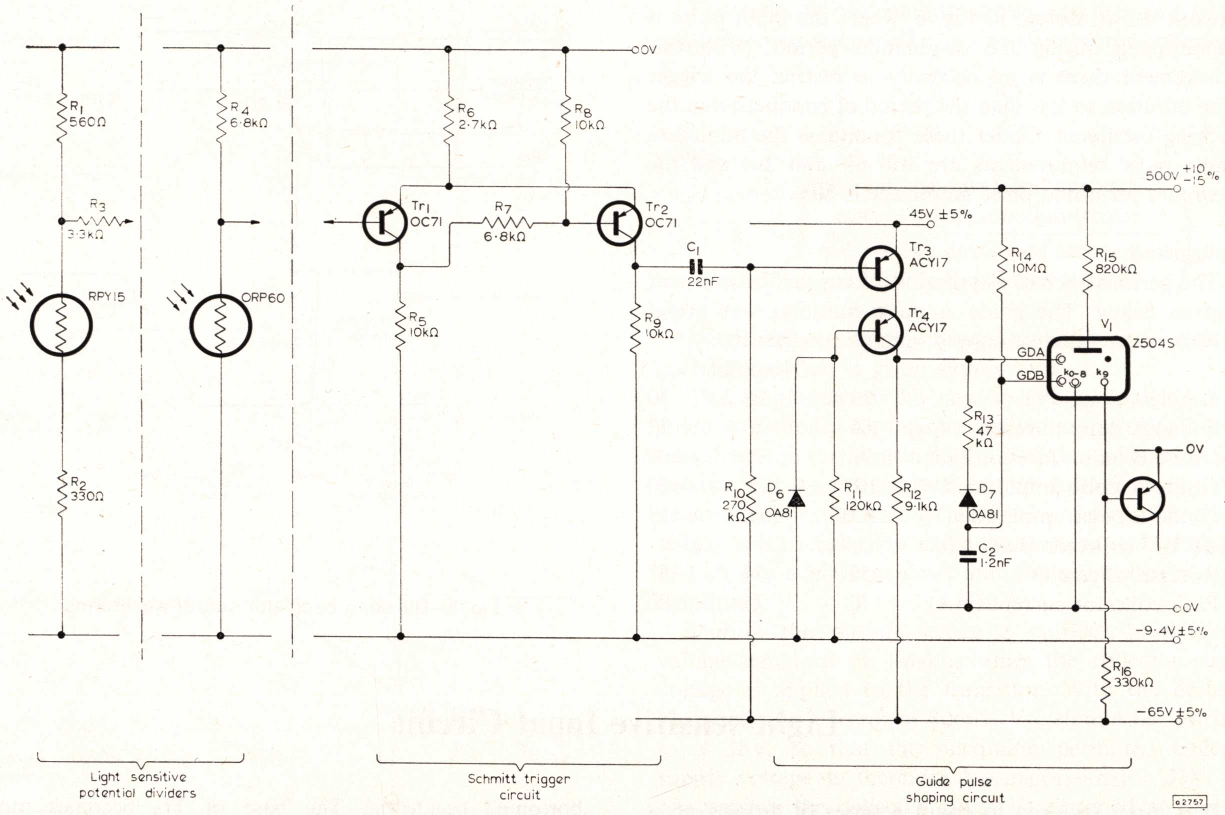

R1 560Ω
R3 3·3kΩ
RPY15
R2 330Ω
R4 6·8kΩ
ORP60
Tr1 OC71
R6 2·7kΩ
R7 6·8kΩ
R8 10kΩ
Tr2 OC71
R5 10kΩ
R9 10kΩ
0V
C1 22nF
500V +10% −15%
45V ±5%
Tr3 ACY17
Tr4 ACY17
R14 10MΩ
R15 820kΩ
V1 Z504S
GDA
GDB
R13 47kΩ
R10 270kΩ
D6 OA81
R11 120kΩ
R12 9·1kΩ
D7 OA81
C2 1·2nF
0V
−9·4V±5%
R16 330kΩ
−65V±5%
Light sensitive potential dividers
Schmitt trigger circuit
Guide pulse shaping circuit
A2757

Fig. 9—Light-sensitive input circuit

TABLE 1

Performance of the Light-sensitive Circuit

	ORP60	RPY15
Cell sensitive area	0·2cm²	1·25cm²
Cell illumination	≥ 2000 lux	≥ 1000 lux
'Dark' background level	≤ 10 lux	≤ 10 lux
Minimum obscuration time	14ms	14ms
Minimum recovery between successive obscurations	26ms	60ms
Maximum operating speed	25c/s	13c/s

The ORP60 network shown in Fig. 9 is designed to operate at an illumination level of ≥ 2000 lux, falling to a background level of ≤ 10 lux when the light is obscured by the object to be counted. This cell has the advantage of small size and can be used to sense small objects at counting speeds up to at least 25c/s. The RPY15 circuit is included for use in cases where an illumination of 2000 lux is not available. However, because of the reduced level of illumination this arrangement operates only at speeds up to approximately 13c/s.

The maximum counting speeds given in Table 1 have been calculated from the worst expected rise and fall time characteristics of the cells, together with the worst limit component and supply voltage variations. At the start of life, the circuits will operate at speeds considerably in excess of the figures quoted.

Auxiliary Circuits

Two possible arrangements of the circuits described earlier are given in Figs. 10 and 11. In the first case a 0 to 4000 p.p.s. triggered blocking oscillator drives the first tube in the counting chain, and in the second case the light-sensitive input circuit is used. These circuits also require a source of supply voltage and a system for resetting the count to zero.

POWER SUPPLY

To simplify and reduce the cost of the power supplies, the potentials in Figs. 10 and 11 have been reduced by 45V so that the original positive guide voltage line is at zero potential and all the low-voltage high-current supplies become negative and can be derived from a common source.

The voltage and current levels required for a six decade scaler using either form of input drive circuit are shown in Table 2.

When these power supplies are not readily available, the power supply design given in Fig. 12 may be used.

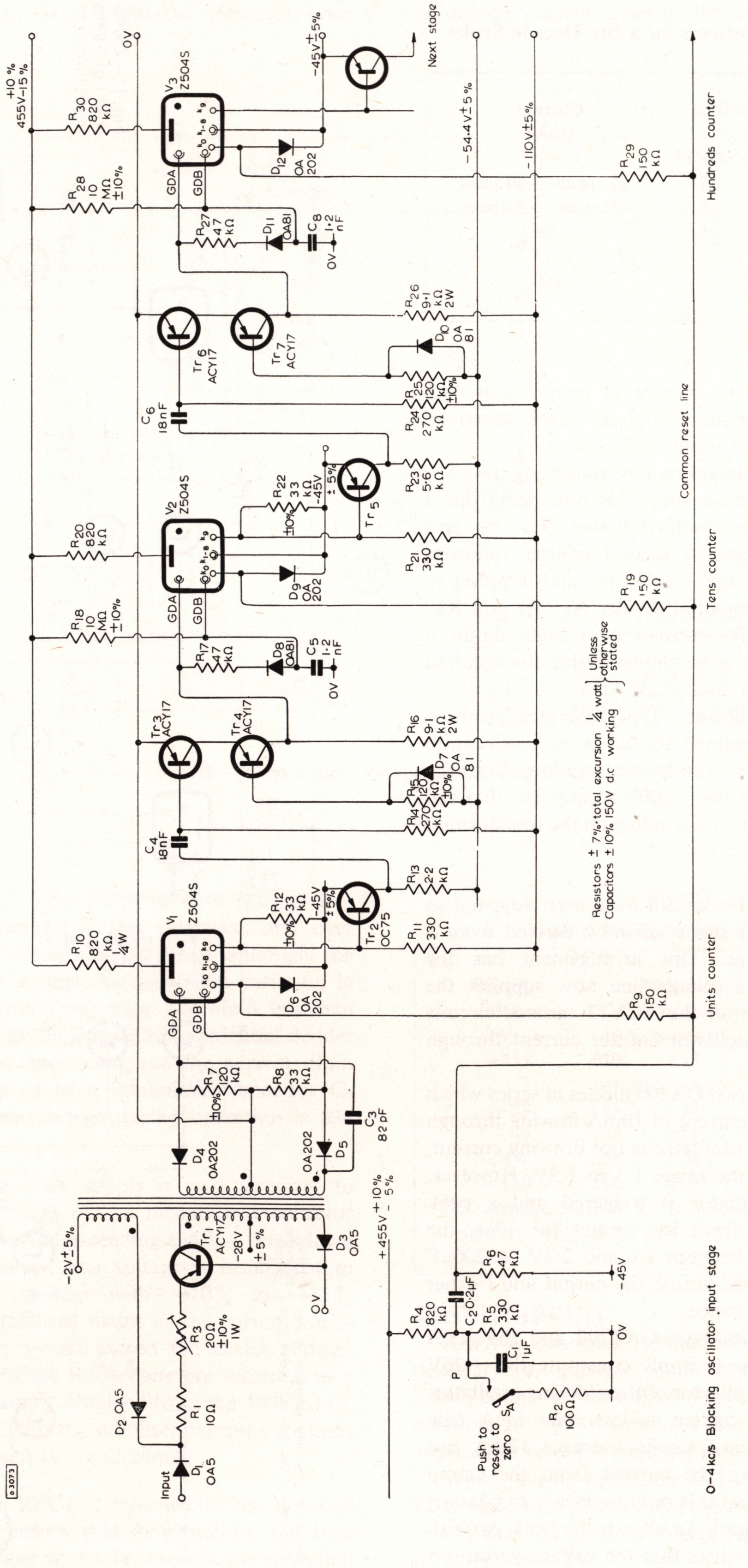

+10% 455V −15%
0V
V3 Z504S
−45V ±5%
Next stage
−54·4V ±5%
−110V ±5%
Hundreds counter
R29 150kΩ
R30 820kΩ
R28 10MΩ ±10%
R27 47kΩ
D11 OA81
C8 1·2nF
D12 OA202
Tr6 ACY17
Tr7 ACY17
R26 9·1kΩ 2W
D10 OA81
C6 18nF
R25 120kΩ ±10%
R24 270kΩ
R23 56kΩ
R22 33kΩ ±10%
Tr5
Common reset line
V2 Z504S
R20 820kΩ
R21 330kΩ
D9 OA202
R18 10MΩ ±10%
R17 47kΩ
D8 OA81
C5 1·2nF
Tens counter
R19 150kΩ
Unless otherwise stated
Resistors ± 7% total excursion ¼ watt
Capacitors ± 10% 150V d.c. working
Tr3 ACY17
Tr4 ACY17
R16 9·1kΩ 2W
D7 OA81
R15 120kΩ ±10%
R14 270kΩ
C4 18nF
R13 22kΩ
R12 33kΩ ±10%
Tr2 OC75
V1 Z504S
R10 820kΩ ¼W
R11 330kΩ
D6 OA202
Units counter
R9 150kΩ
R7 120kΩ ±10%
R8 33kΩ
C3 82pF
D4 OA202
D5 OA202
+455V +10% −5%
Tr1 ACY17
−28V ±5%
D3 OA5
0V
−2V ±5%
R3 20Ω ±10% 1W
D2 OA5
R1 10Ω
D1 OA5
Input
R4 820kΩ
C2 0·2µF
R5 330kΩ
R6 47kΩ
C1 1µF
−45V
0V
P
SA
Push to reset to zero
R2 100Ω
0–4kc/s Blocking oscillator input stage
A3073

Fig. 10—Z504S scaler with 0 to 4000 p.p.s. input circuit and reset facilities

TABLE 2

Supply Voltage Requirements for a Six Decade Scaler

Supply Voltage (V)	Tolerance (%)	Current (mA)
+455	+10−15	+3
−2	±5	+22 mean +80 peak
−28	±5	−8 mean −80 peak
−45	±5	−26
−54·4	±5	−13
−110	±5	−60

This design is intended to operate in conjunction with up to five of the transistor coupling stages described earlier and either form of input drive circuit.

As all the negative voltages require stabilising to ±5% over life, the most negative supply is obtained from a 108C1 stabiliser with an emitter-follower, Tr_1, to give the desired current range. A second emitter follower, Tr_2, is used to generate the −54V line, and is preset to this value by the base potential divider R_7, R_8 and R_9. The emitter circuit of Tr_2 consists of a zener diode, a resistor and three further zener diodes giving the required voltages of −45V, −28V and −2V.

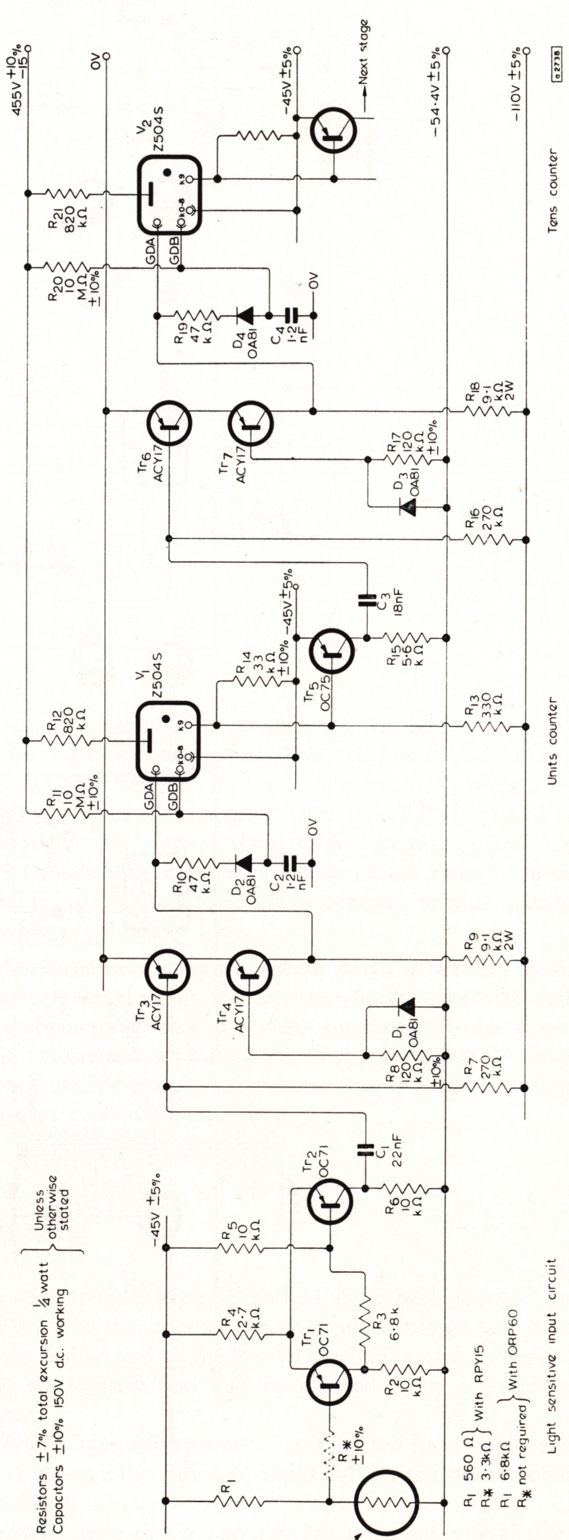
The first emitter-follower, Tr_1, operates from a nominal −145V line obtained by full wave rectification from a 130–0–130V r.m.s. transformer winding. Both the positive 455V supply and the −200V supply are obtained from an additional 390V r.m.s. winding on the transformer.

Design Considerations

The voltage levels in the circuit have been adjusted so that all the high current loads are now derived from a common negative source. This arrangement has the advantage that the zero voltage line now supplies the 60mA emitter current to all the ACY17 cascode circuits and also the blocking oscillator emitter current through the −2V line.

The −2V circuit uses two OA200 diodes in series which are forward biased by a current of 10mA flowing through R_{11}. When the blocking oscillator is not drawing current, the output voltage is in the range 1·3 to 1·9V. However, when the blocking oscillator is triggered and a peak current of 80mA flows from this circuit for 70μs, the voltage can only rise to between 1·6 and 2·3V. A 200μF capacitor, C_7, is connected across the output and further reduces the output impedance.

The three zener diodes type OAZ207 and the 390Ω resistor, R_{10}, in the power supply constitute the −26V to −30V supply for the collector of the blocking oscillator. As the mean collector current is less than 8mA (the current during the forward stroke averages 12mA but during the reverse stroke the current from the clamp winding reduces this figure) it is only necessary to connect a capacitor across the supply to absorb the peak current. A 64μF capacitor, C_6, ensures that the voltage variations at the output terminal are less than 2V.

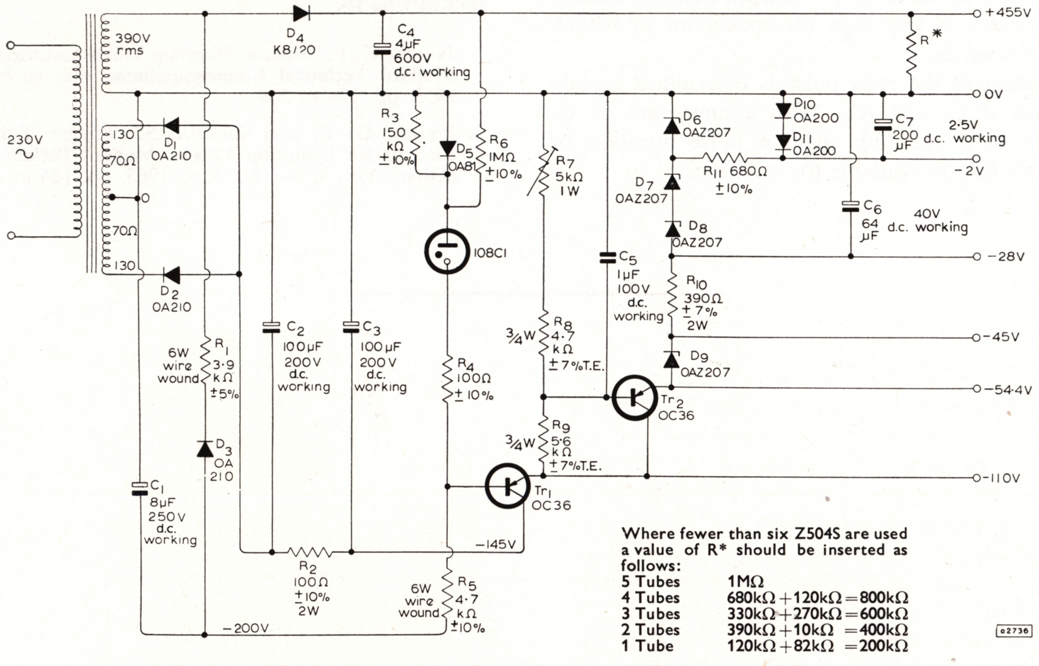

455V +10% −15%
0V
−45V ±5%
−54·4V ±5%
−110V ±5%
V2 Z504S
V1 Z504S
GDA
GDB
R21 820 kΩ
R20 10 MΩ ±10%
R19 47 kΩ
D4 OA81
C4 12 nF
0V
Next stage
Tr6 ACY17
Tr7 ACY17
R18 9·1 kΩ 2W
R17 120 kΩ ±10%
D3 OA81
R16 270 kΩ
C3 18nF
Tr5 OC75
R14 33 kΩ ±10%
R15 5·6 kΩ
R13 330 kΩ
R12 820 kΩ
R11 10 MΩ ±10%
R10 47 kΩ
D2 OA81
C2 12 nF
Tr3 ACY17
Tr4 ACY17
R9 9·1 kΩ 2W
D1 OA81
R8 120 kΩ ±10%
R7 270 kΩ
Tens counter
Units counter
Tr2 OC71
C1 22nF
R6 10 kΩ
R5 10 kΩ
R4 2·7 kΩ
R3 6·8 k
Tr1 OC71
R2 10 kΩ
R* ±10%
R1
Light sensitive input circuit

Resistors ±7% total excursion ¼ watt
Capacitors ±10% 150V d.c. working } Unless otherwise stated

R_1 560 Ω
R_* 3·3kΩ } With RPY15
R_1 6·8kΩ
R_* not required } With ORP60

Fig. 11—Z504S scaler with light-sensitive input circuit

The emitter-follower Tr_2 is required to supply a current in the range 36 to 72mA, depending upon the zener voltages of diodes D_6, D_7, D_8 and D_9. However, once the circuit is preset to −54V with variable resistor R_7, the load current variations during operation and over life are unlikely to exceed 20mA. Thus although the standing base current is high, the maximum variation in base current due to circuit operation and life is less than 600μA. A relatively high impedance base potential divider network has therefore been used and the current drain in this network reduced to a minimum. Capacitor C_5 ensures that the ripple voltage during operation is less than 2V.


390V r.m.s
230V ~
130
70Ω
70Ω
130
D4 K8/20
C4 4μF 600V d.c. working
+455V
R*
0V
D1 OA210
D2 OA210
R3 150 kΩ ±10%
D5 OA81
R6 1MΩ ±10%
R7 5kΩ 1W
108C1
D6 OAZ207
D7 OAZ207
D8 OAZ207
D9 OAZ207
D10 OA200
D11 OA200
R11 680Ω ±10%
C7 200 μF 2·5V d.c. working
−2V
C6 64 μF 40V d.c. working
−28V
C5 1μF 100V d.c. working
R10 390Ω ±7% 2W
−45V
−54·4V
−110V
R8 4·7 kΩ ±7%T.E. ¾W
R9 5·6 kΩ ±7%T.E. ¾W
Tr2 OC36
Tr1 OC36
6W wire wound R1 3·9 kΩ ±5%
D3 OA 210
C2 100μF 200V d.c. working
C3 100μF 200V d.c. working
R4 100Ω ±10%
C1 8μF 250V d.c. working
R2 100Ω ±10% 2W
−145V
6W wire wound R5 4·7 kΩ ±10%
−200V

Where fewer than six Z504S are used a value of R* should be inserted as follows:

5 Tubes	1MΩ
4 Tubes	680kΩ+120kΩ=800kΩ
3 Tubes	330kΩ+270kΩ=600kΩ
2 Tubes	390kΩ+10kΩ =400kΩ
1 Tube	120kΩ+82kΩ =200kΩ

Fig. 12—Power supply for six-decade Z504S scaler

In considering the 110V supply it was necessary to restrict the nominal value of the unstabilised collector supply to −145V, to avoid exceeding the V_{ce} breakdown voltage of Tr_1. However, this voltage is insufficient to operate the 108C1 stabiliser with +10% to −15% variations in the unstabilised mains as the current variations in the stabiliser would exceed the device ratings. The stabiliser load resistor R_5 is therefore returned to a −200V unstabilised supply obtained from the 390V r.m.s. transformer winding. Thus the stabiliser current variations are restricted to between 10·8 and 26mA.

The anode of the 108C1 is returned to the network R_3, R_6 and D_5 to ensure that at switch-on the tube strikes before the voltage across Tr_2 exceeds the permitted V_{ce} rating for the device.

Power Supply Performance

The performance of a typical power supply driving a six decade scaler is given in Table 3.

TABLE 3

Typical Power Supply Performance

Supply Voltage (V)	Mains Input Variation +10%	Nominal	−15%	Peak to Peak Ripple Voltage (V)
+455	510	455	385	10
−2	−1·56	−1·56	−1·55	0·75
−28	−28·5	−28	−27·5	1·3
−45	−45	−45	−44·5	1·7
−54·4	−55	−54·4	−54·4	1·2
−110	−110	−109	−108	3·2

The variable resistor R_7 is adjusted to give the correct nominal voltage at the −54·4V supply terminal.

RESET CIRCUIT

After a counting period has been registered it is necessary to provide some means of resetting each Z504S counting tube either to zero or to a pre-determined position. In Fig. 10 switch S_A and associated components are used to reset the stepping tubes to zero.

When, during operation, a discharge is present at the k_0 cathode in a Z504S tube, the clamp diodes D_6, D_9 etc. ensure that the positive voltage excursion at any cathode is limited to < 1V.

When it is required to reset the counter to zero, switch

S_A is closed and C_1 discharges rapidly through R_2. The potential difference at point P therefore falls rapidly from 166V to 0V and a negative pulse of 166V amplitude is applied to the common reset line by capacitor C_2. This negative pulse is sufficient to cause unprimed breakdown between anode and k_0 in each tube in the chain. Resistors R_9, R_{19} and R_{29} serve to limit the peak cathode current to a value which is less than the maximum of 650μA given in published data.

The duration of the reset pulse is determined mainly by the value of C_2 and R_6. With a maximum of six Z504S tubes in a counting chain a pulse duration of approximately 6ms is available for resetting.

This circuit has the advantage that switch bounce has no effect on the resetting procedure, because if S_A opens momentarily C_1 is recharged slowly by R_4 and R_5.

REFERENCES

1. JEYNES, G. F. 'Decade Stepping Tubes and their Operation'. **Mullard Technical Communications,** Vol. 4, No. 37, Feb. 1959, pp. 194 to 208.
2. JEYNES, G. F. and ZILKHA, S. 'Trigger Tube Coupling Circuits for Counting Tubes'. **Mullard Technical Communications,** Vol. 7, No. 66, Aug. 1963, pp. 184 to 193.